Compal Confidential

HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA G73M/G72MV/NB7P-SE)

2006-10-04
REV: 4.0

Security Classification	Compal Secret Data		
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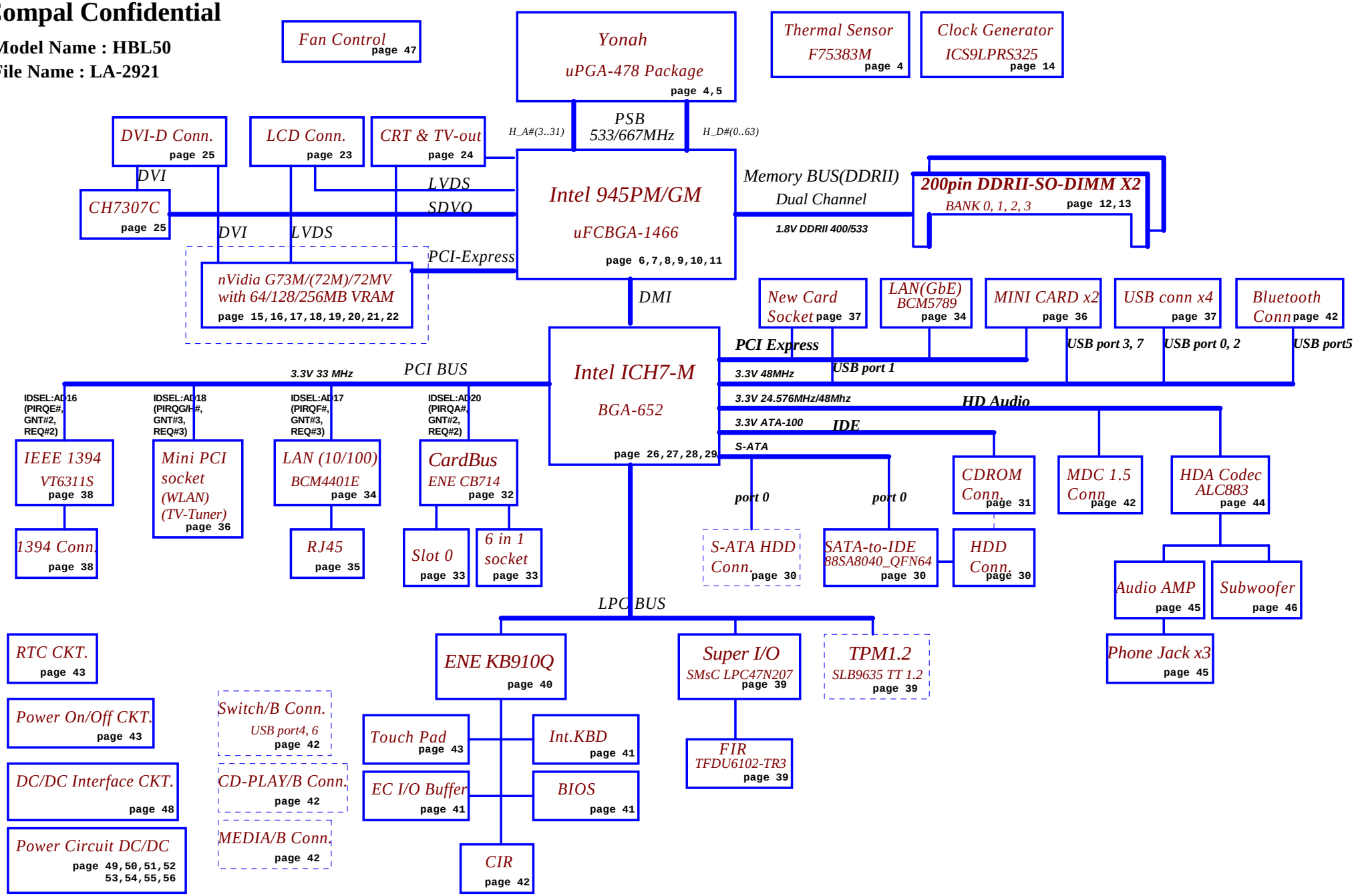
Model Name : HBL50
File Name : LA-2921



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
Fintek F75383M	1001 100X b

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@
CB1410	1410@

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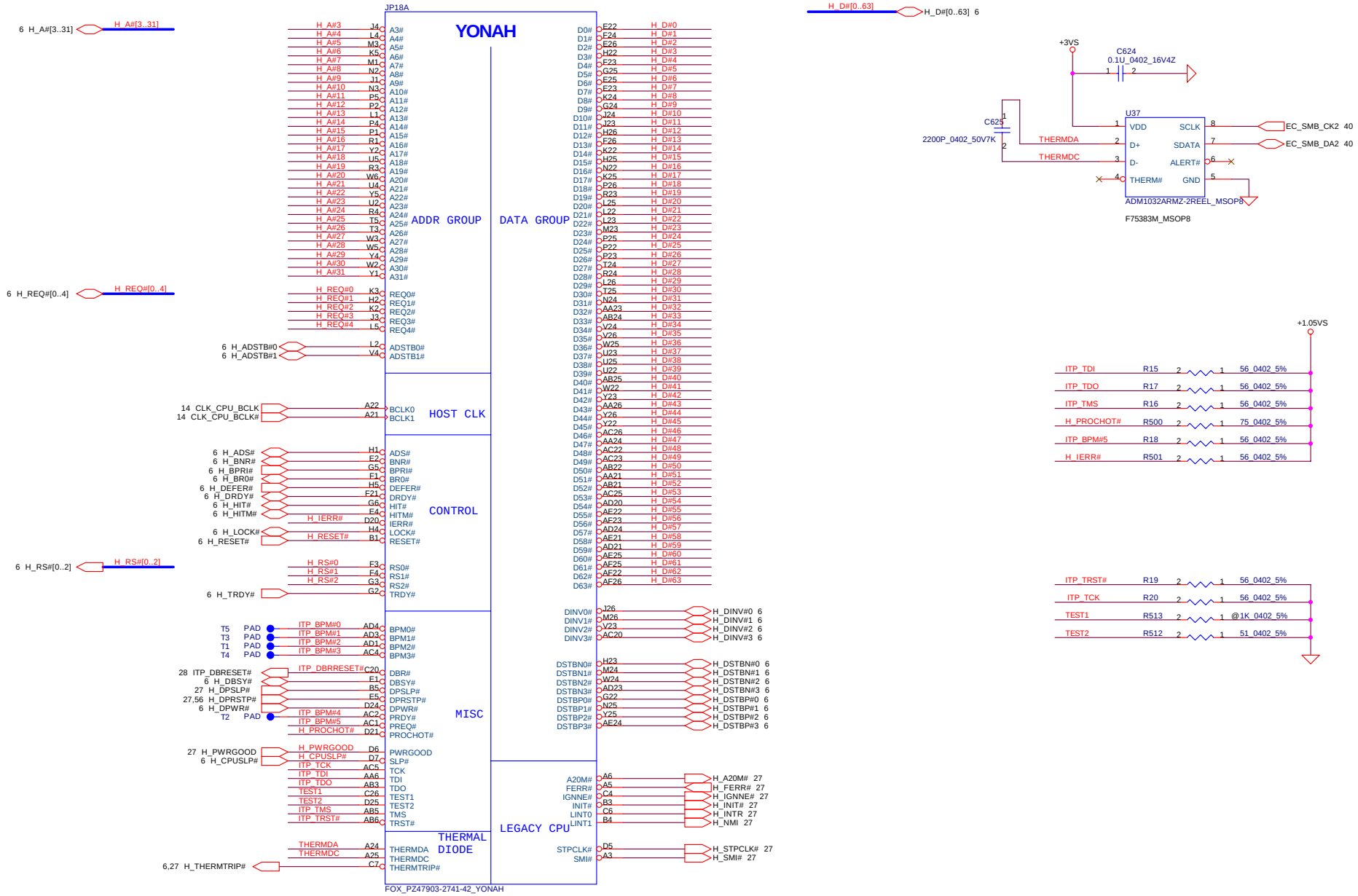

Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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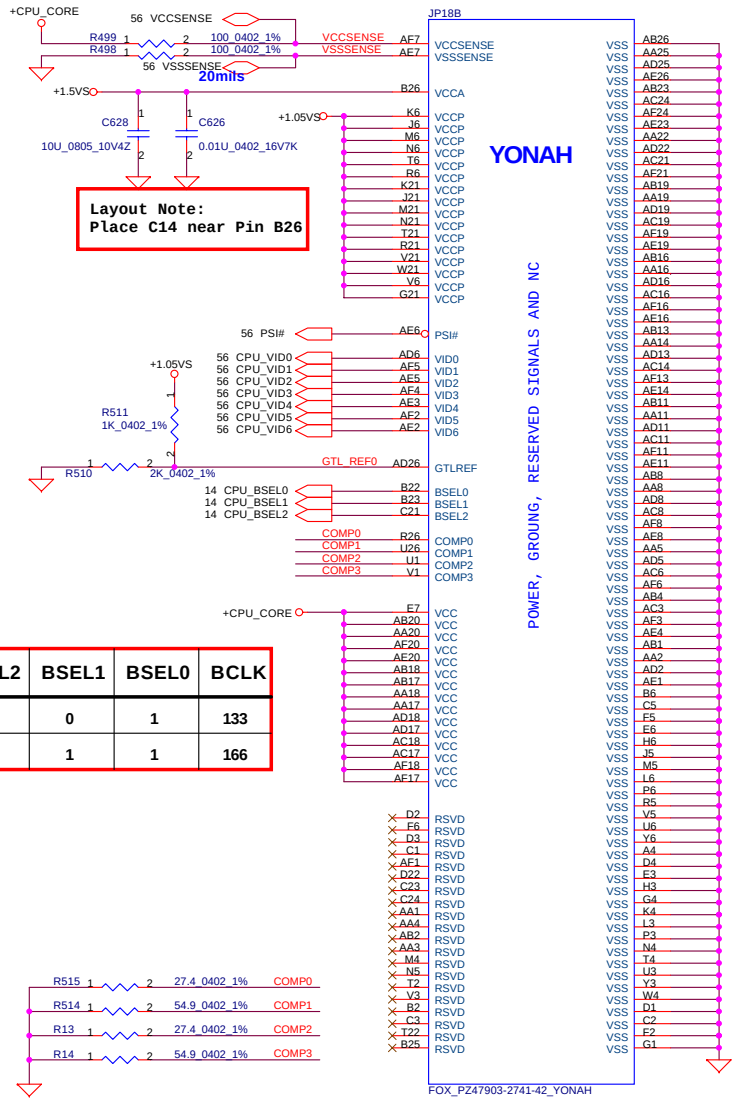
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4Ohms with 50 mil spacing.
Place PU and PD wihin 1 inch of CPU.

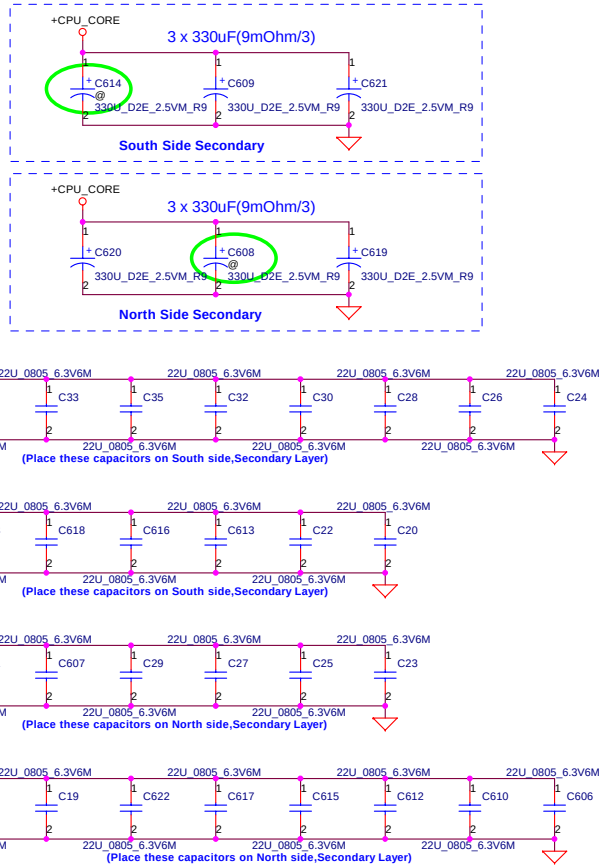


Layout Note:
Place C14 near Pin B26

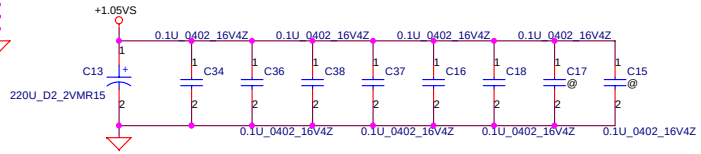
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

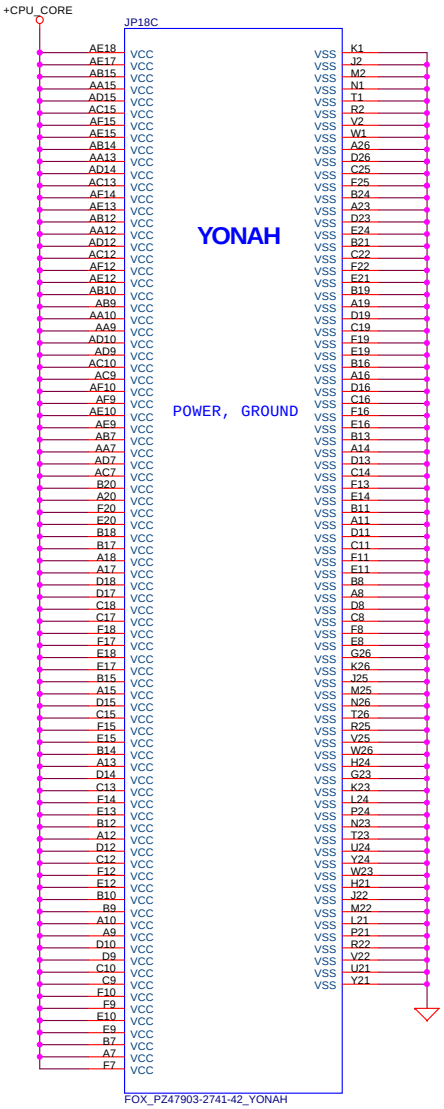
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Space 25mils (55Ohms)



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32





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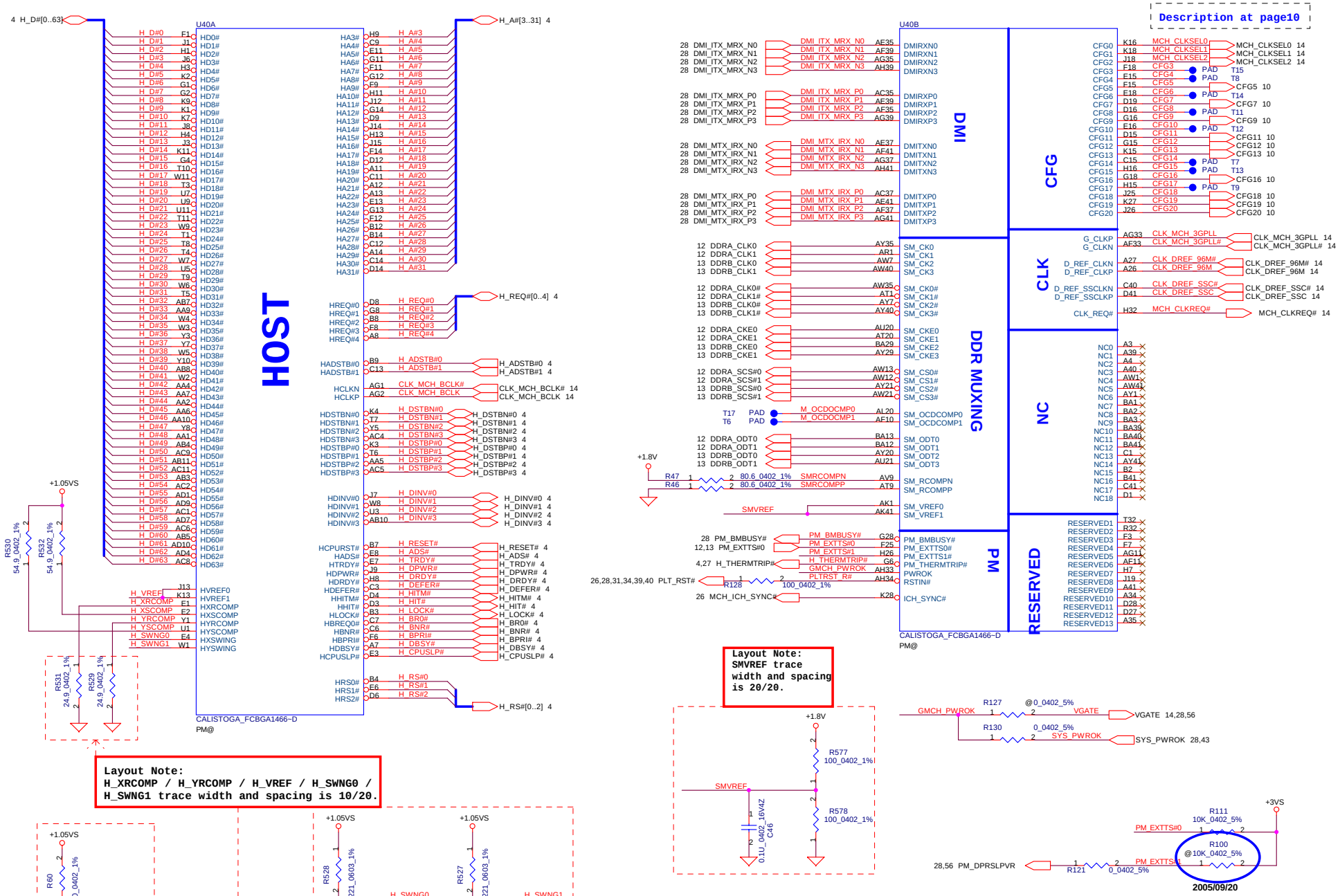
945GM(SL8Z2)[A3]: SA0000059K0(ABO!)
945PM(SL8Z4)[A3]: SA00000KDE0(ABO!)



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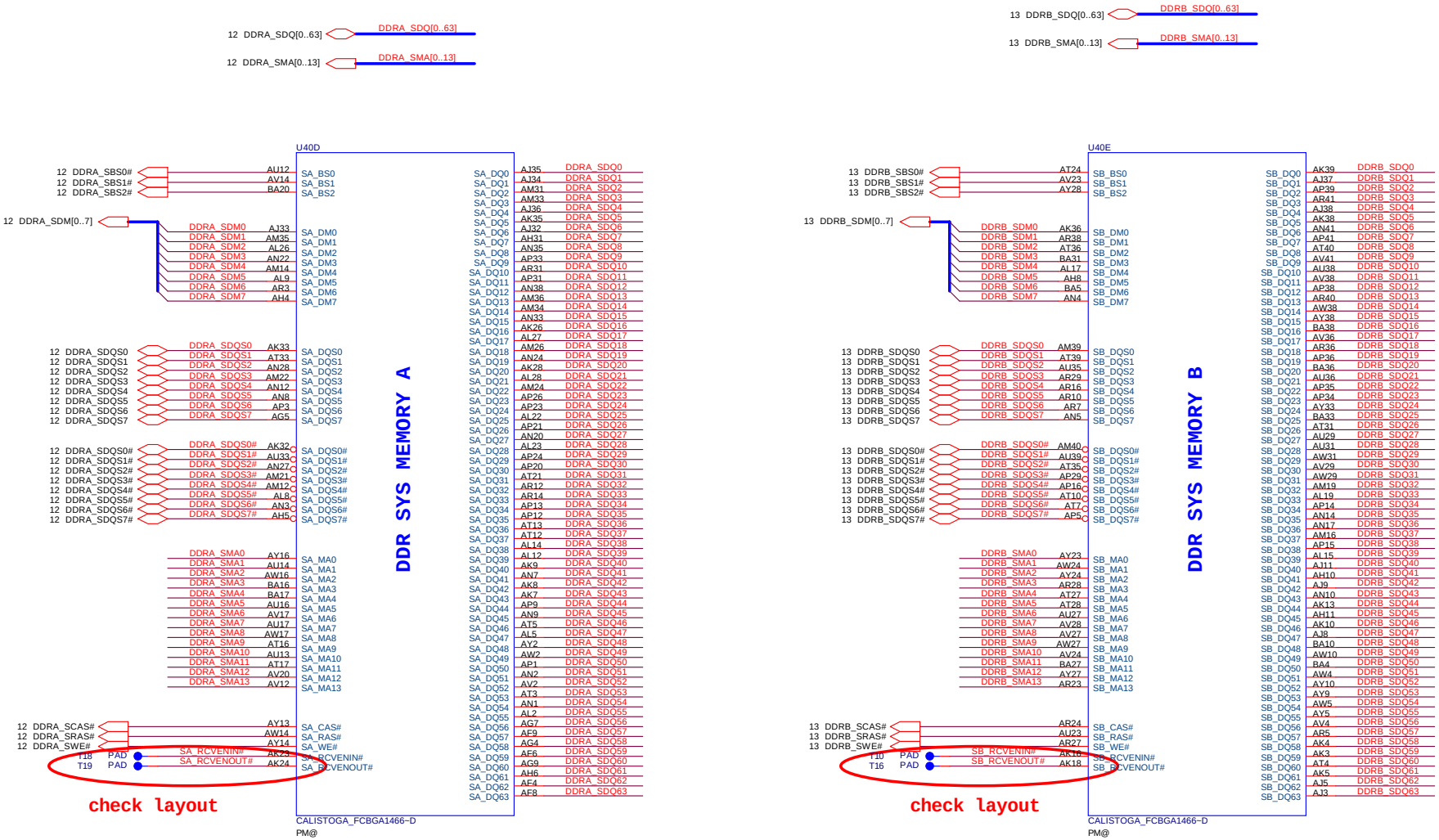

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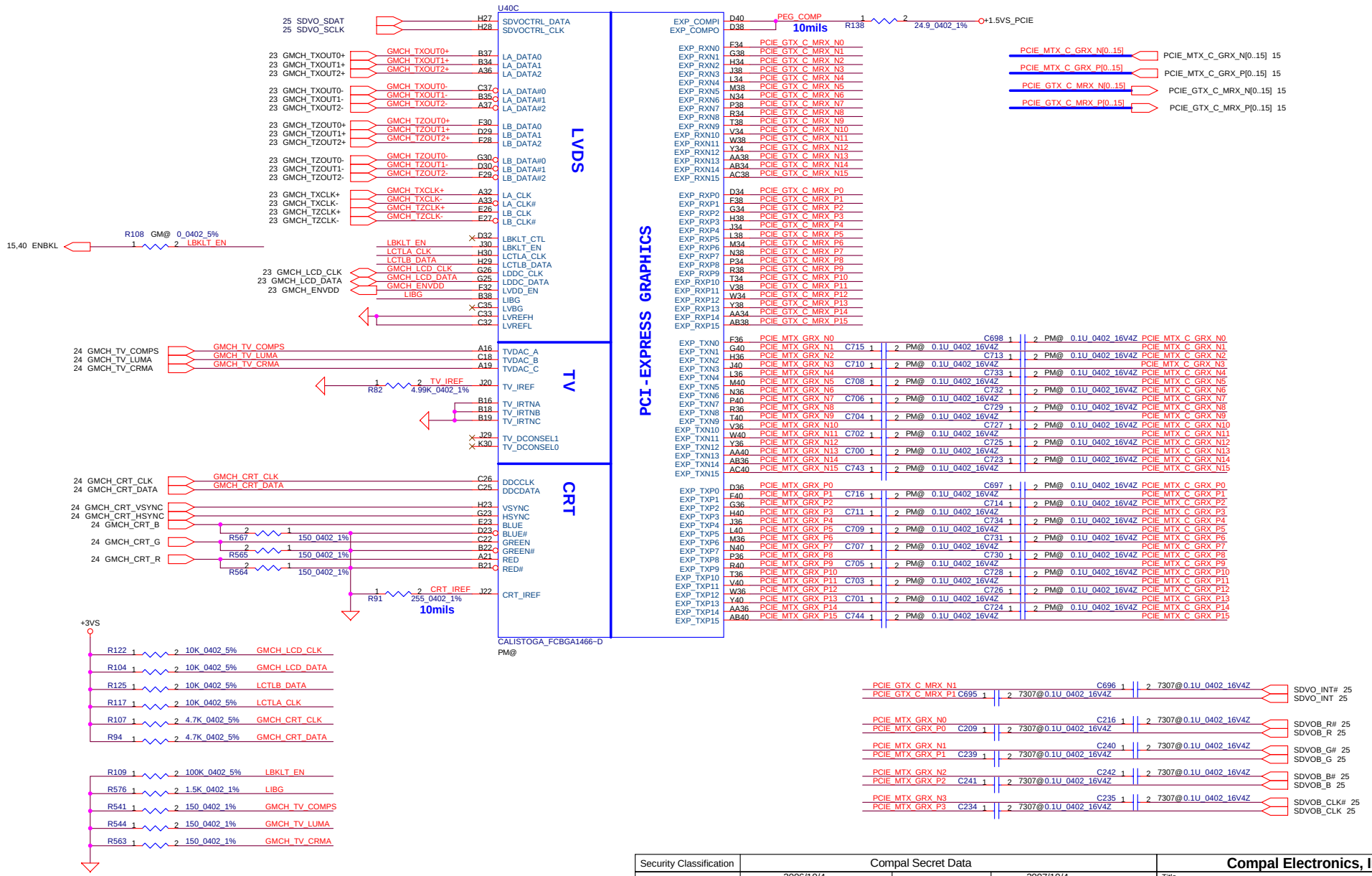

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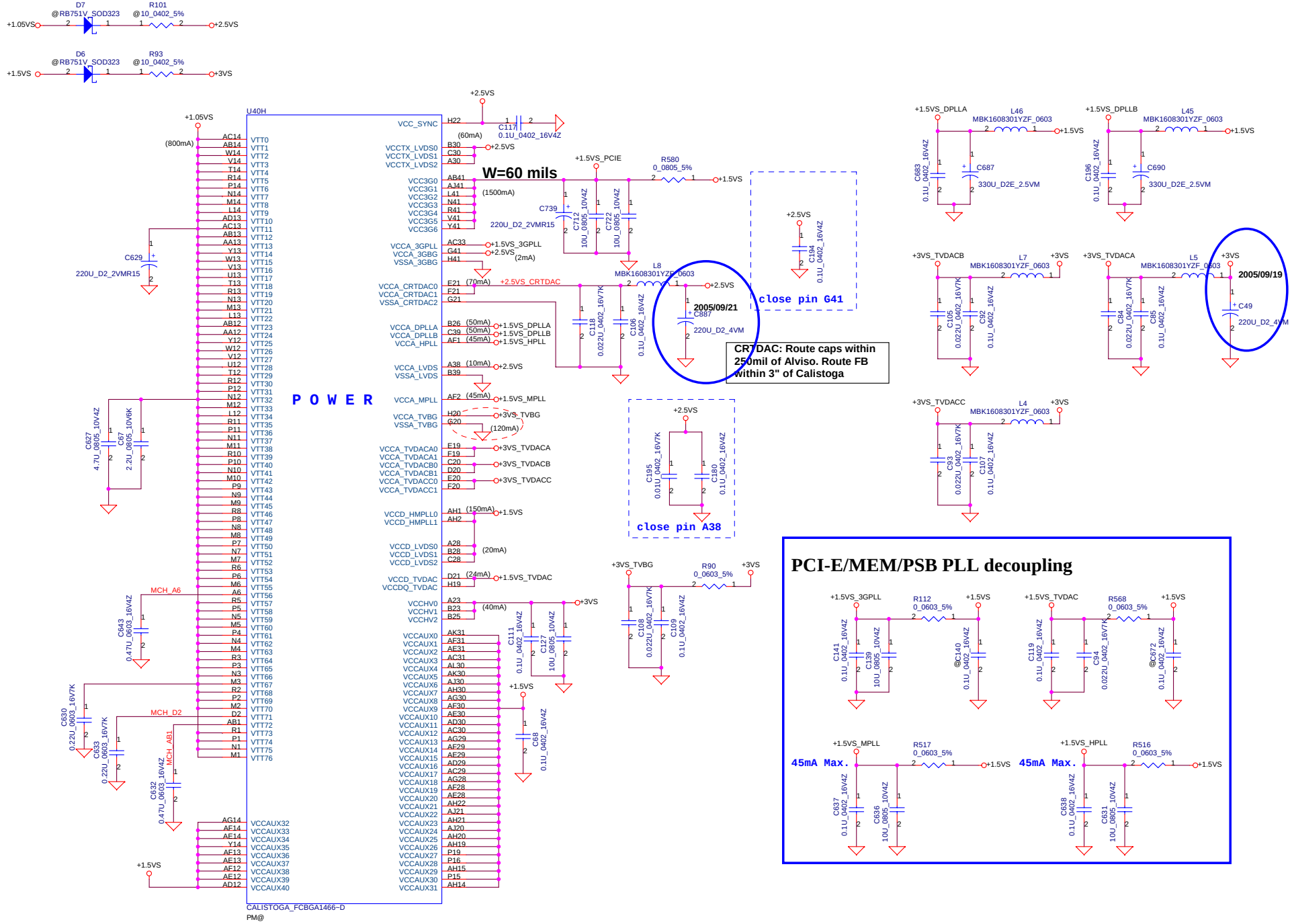

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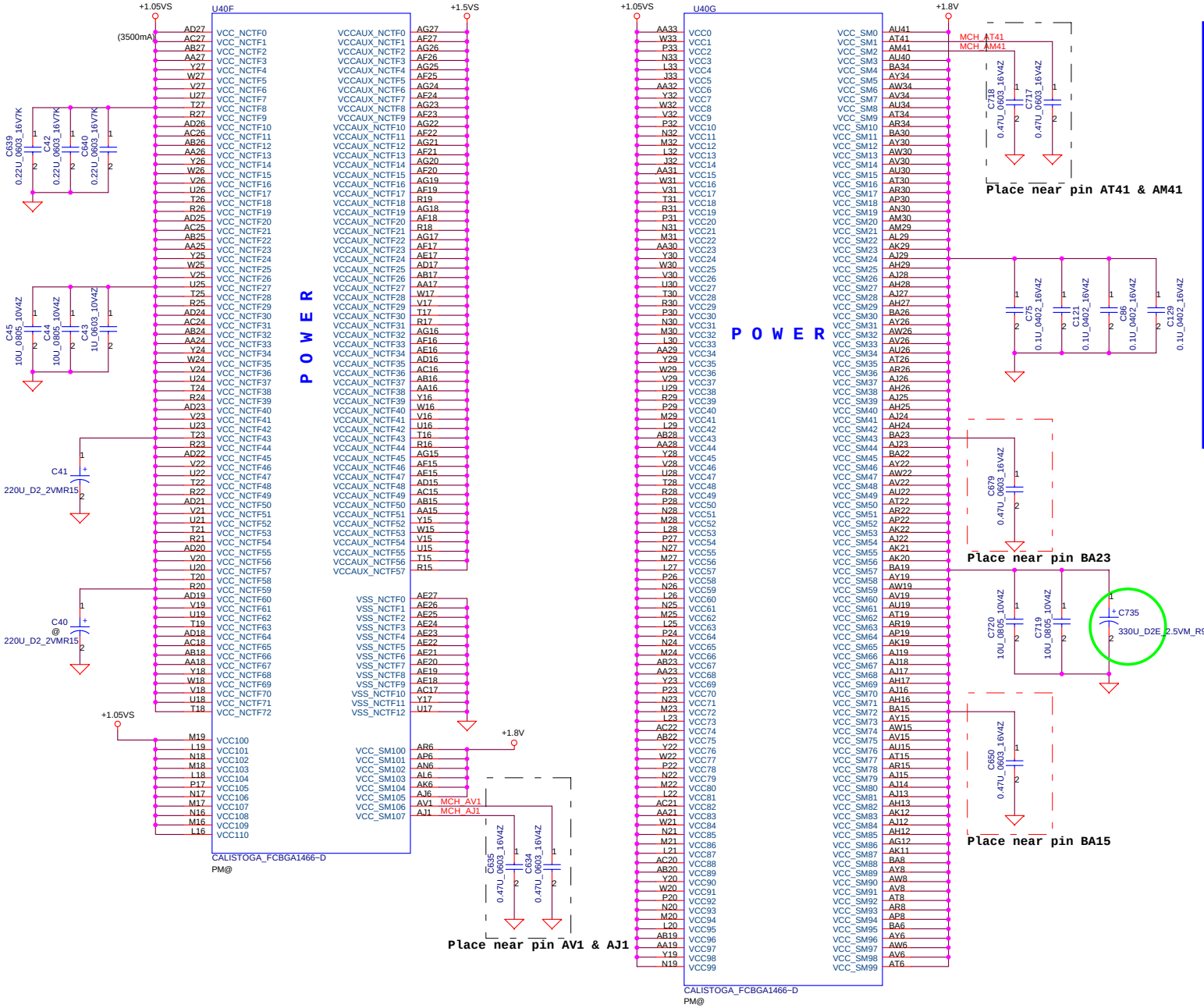
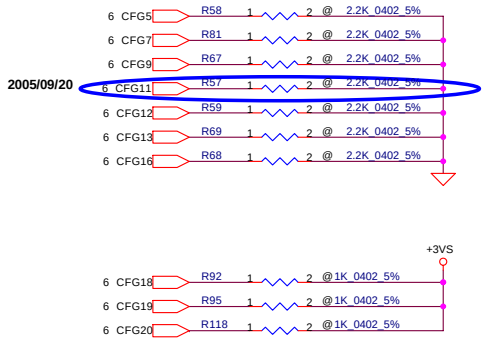


Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



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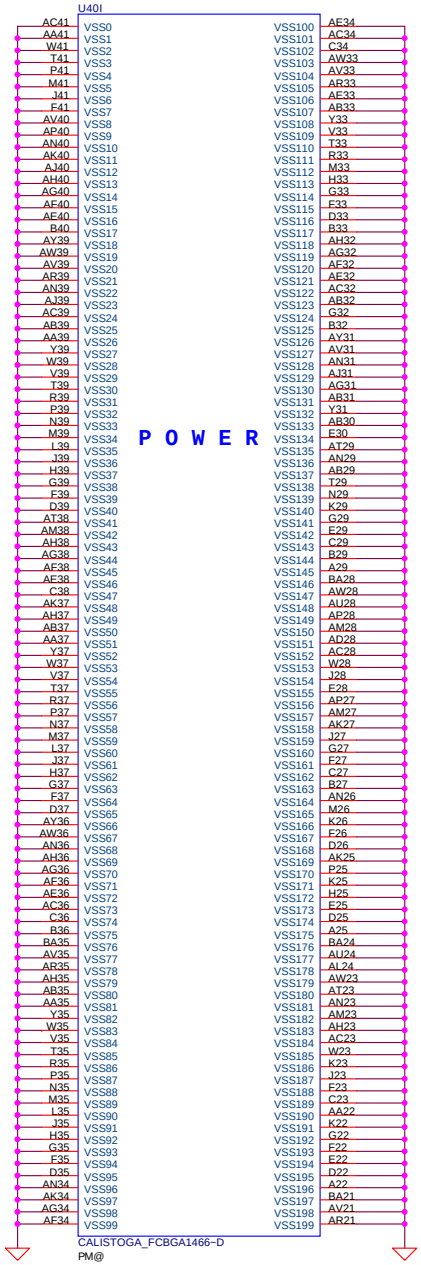

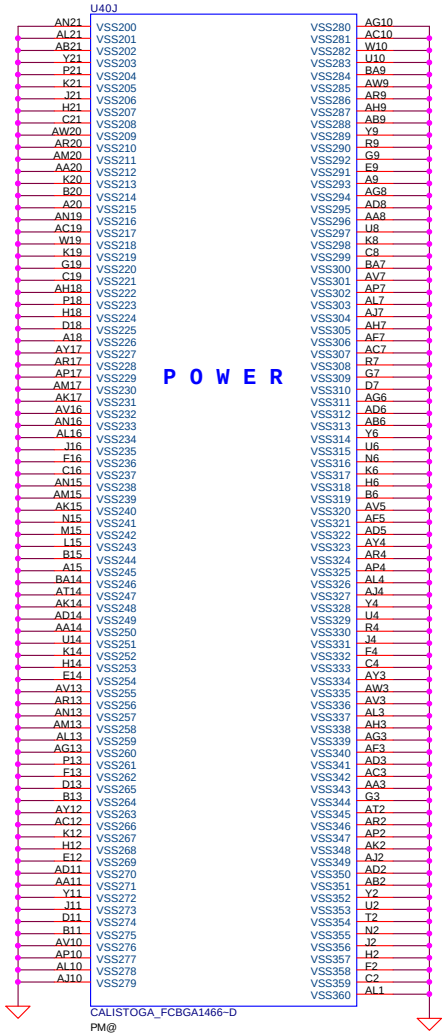

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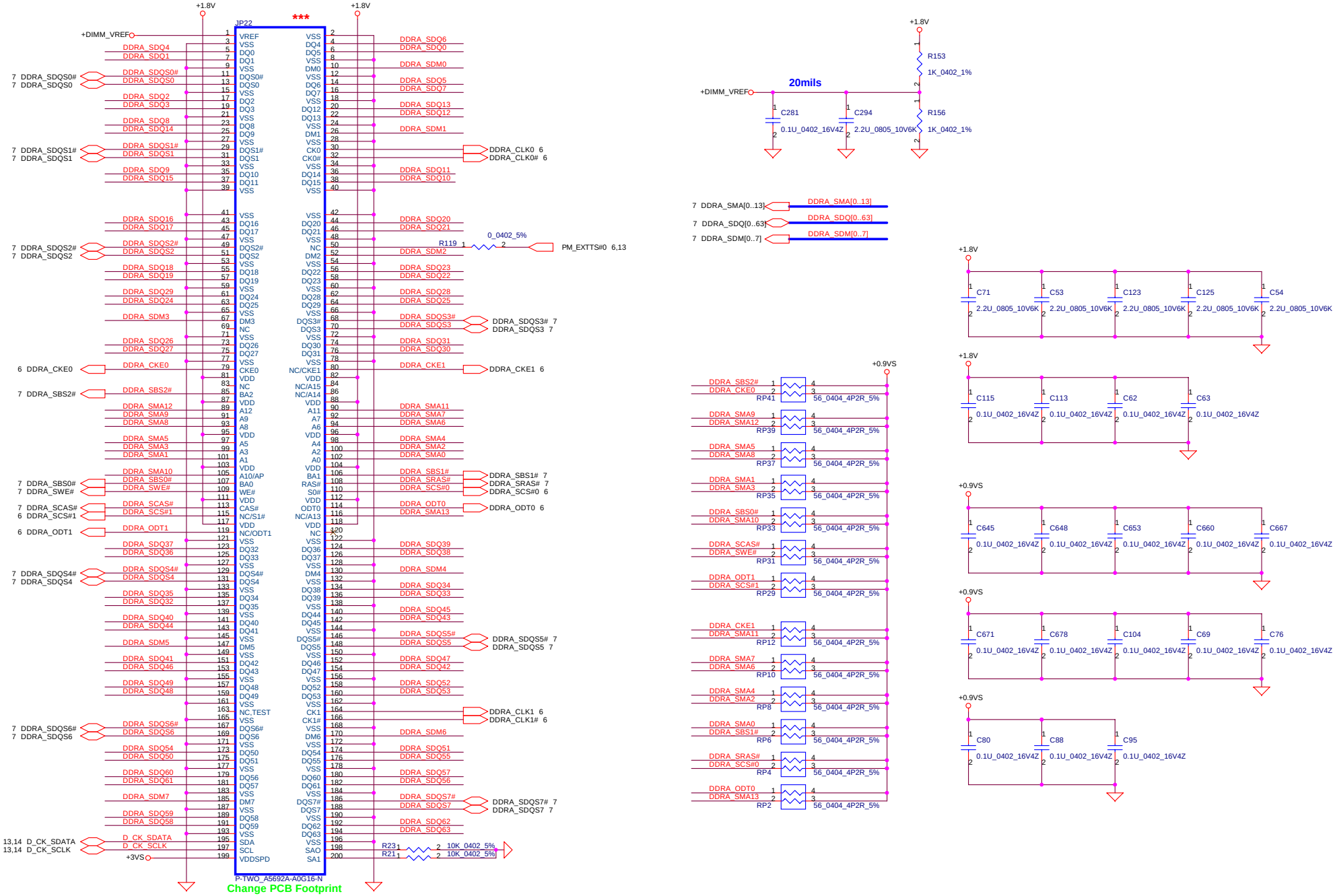

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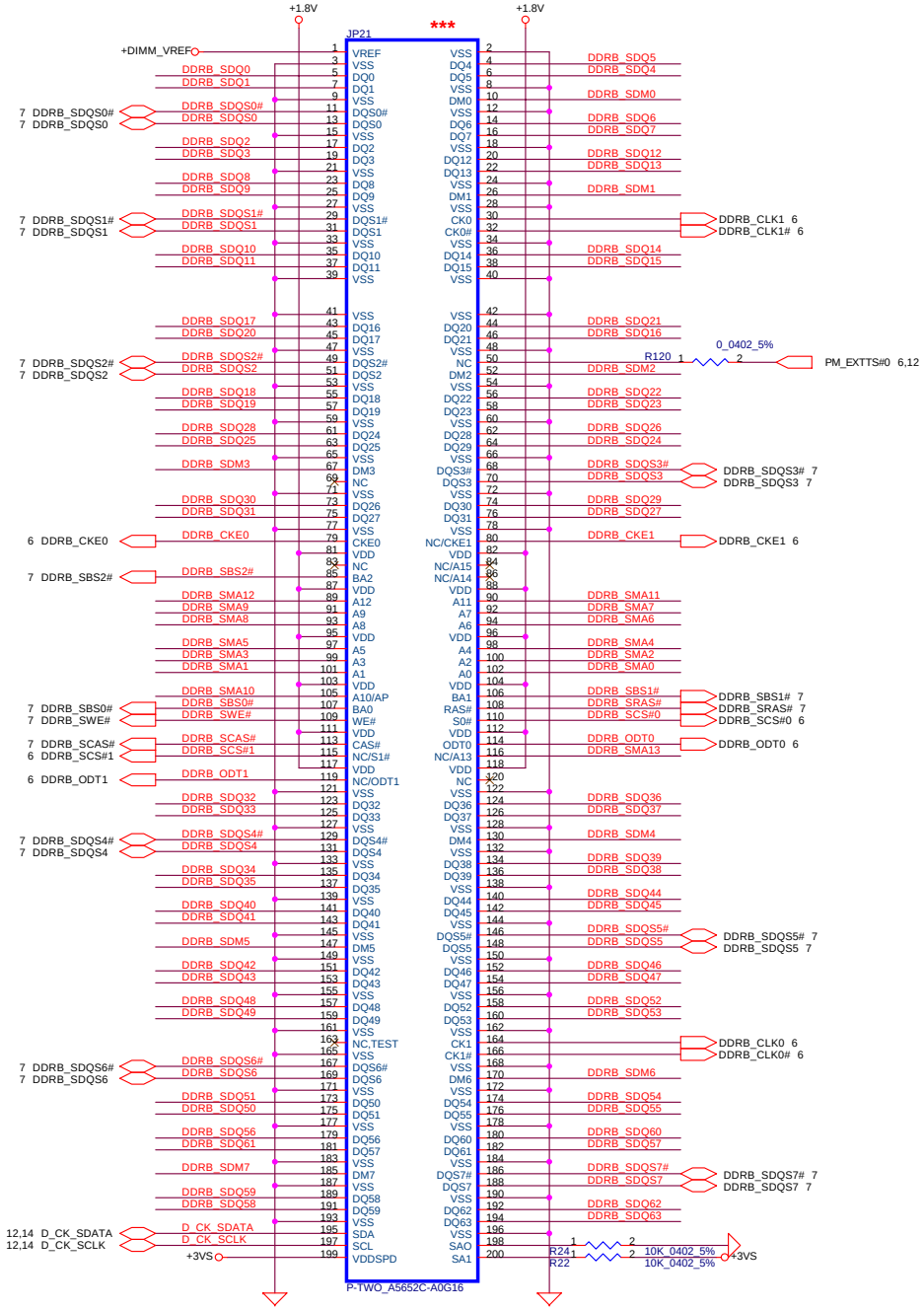

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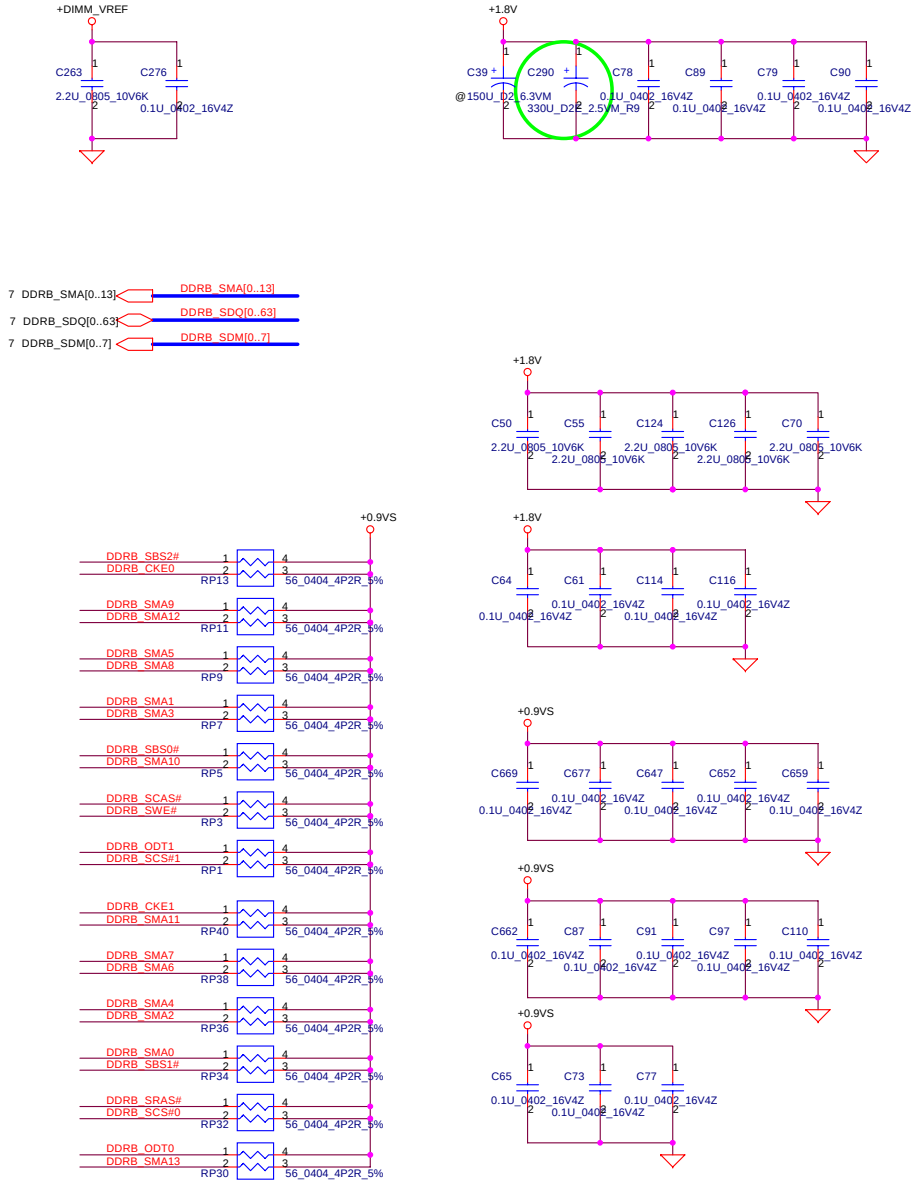

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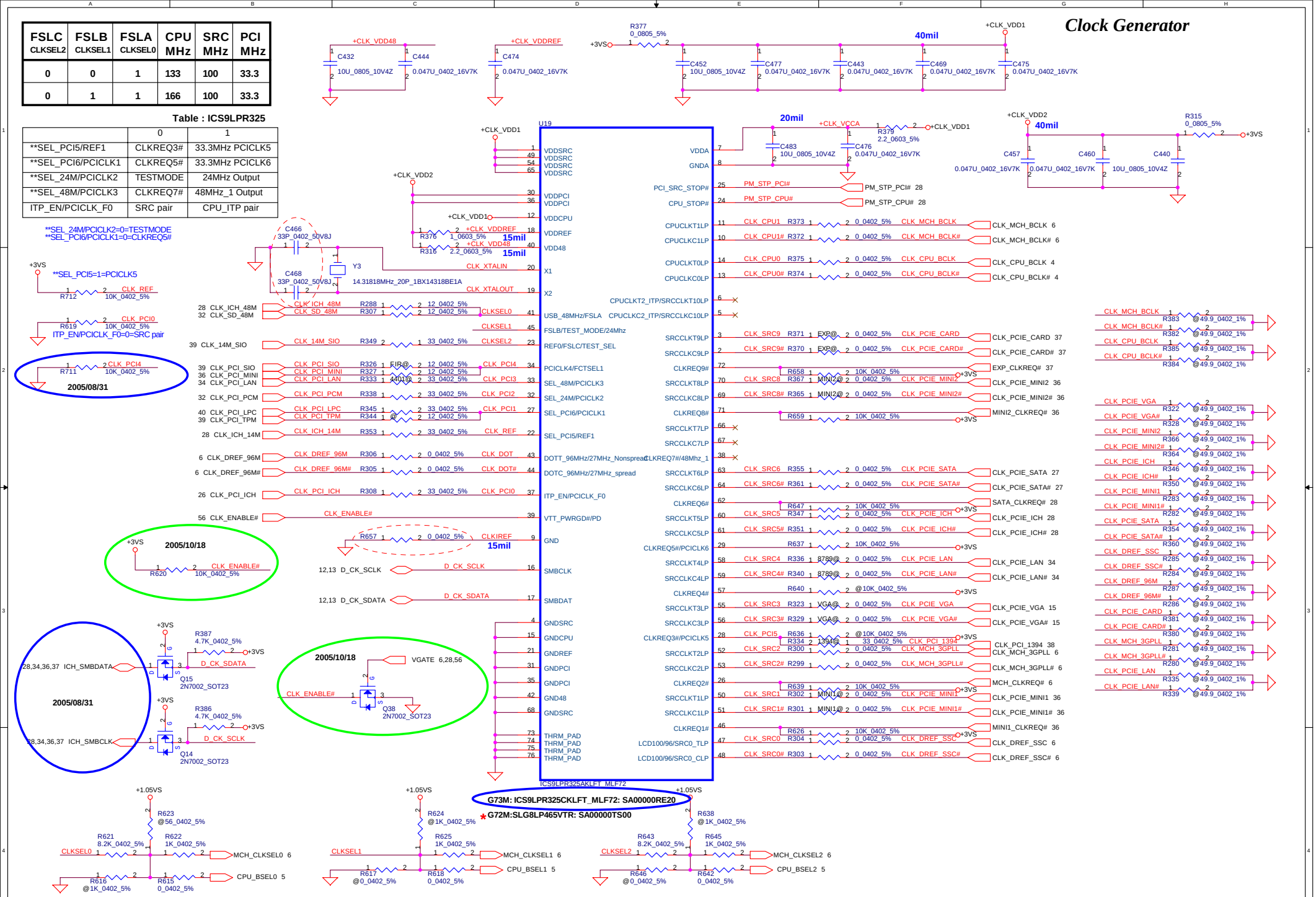
Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair



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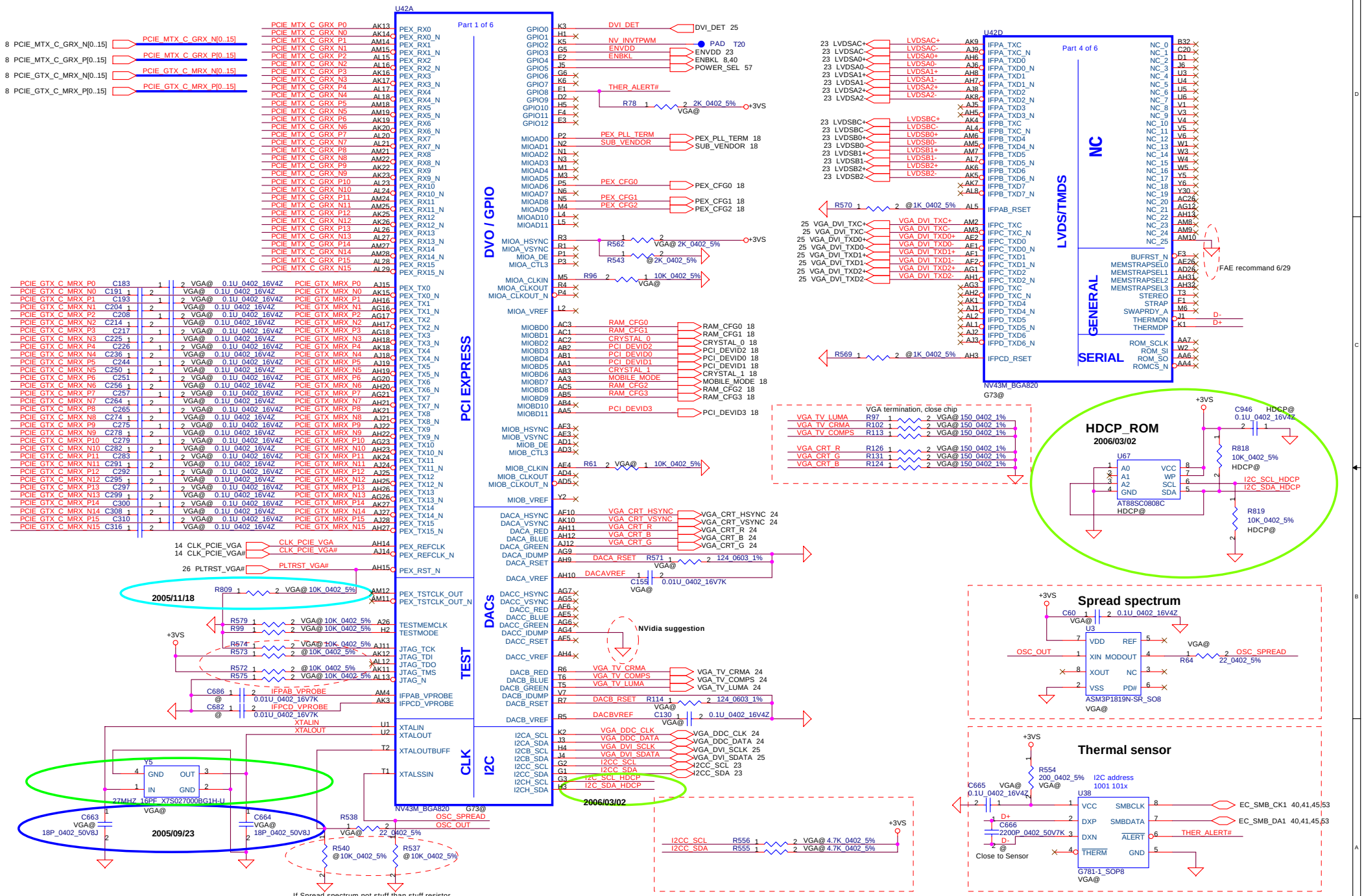

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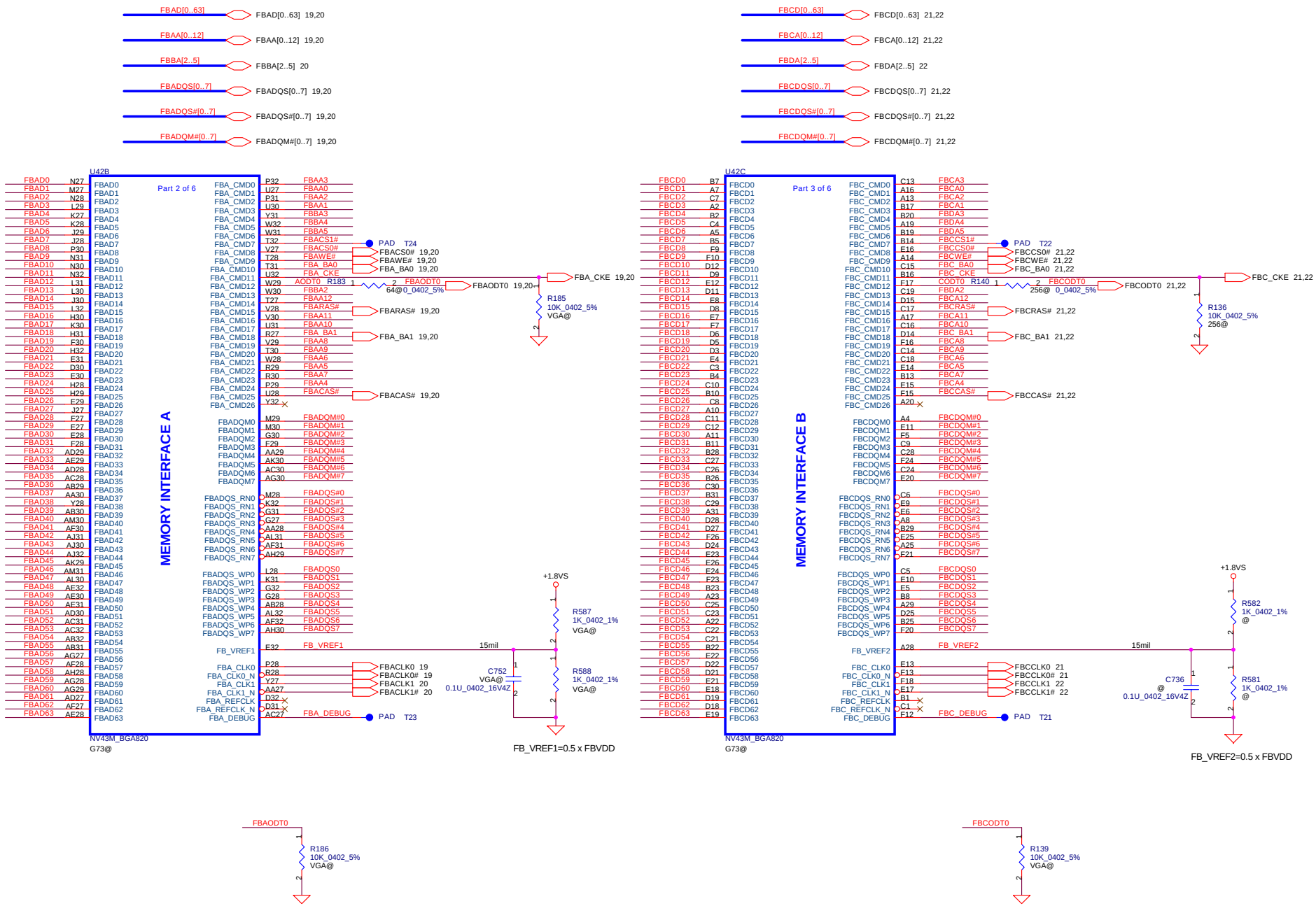

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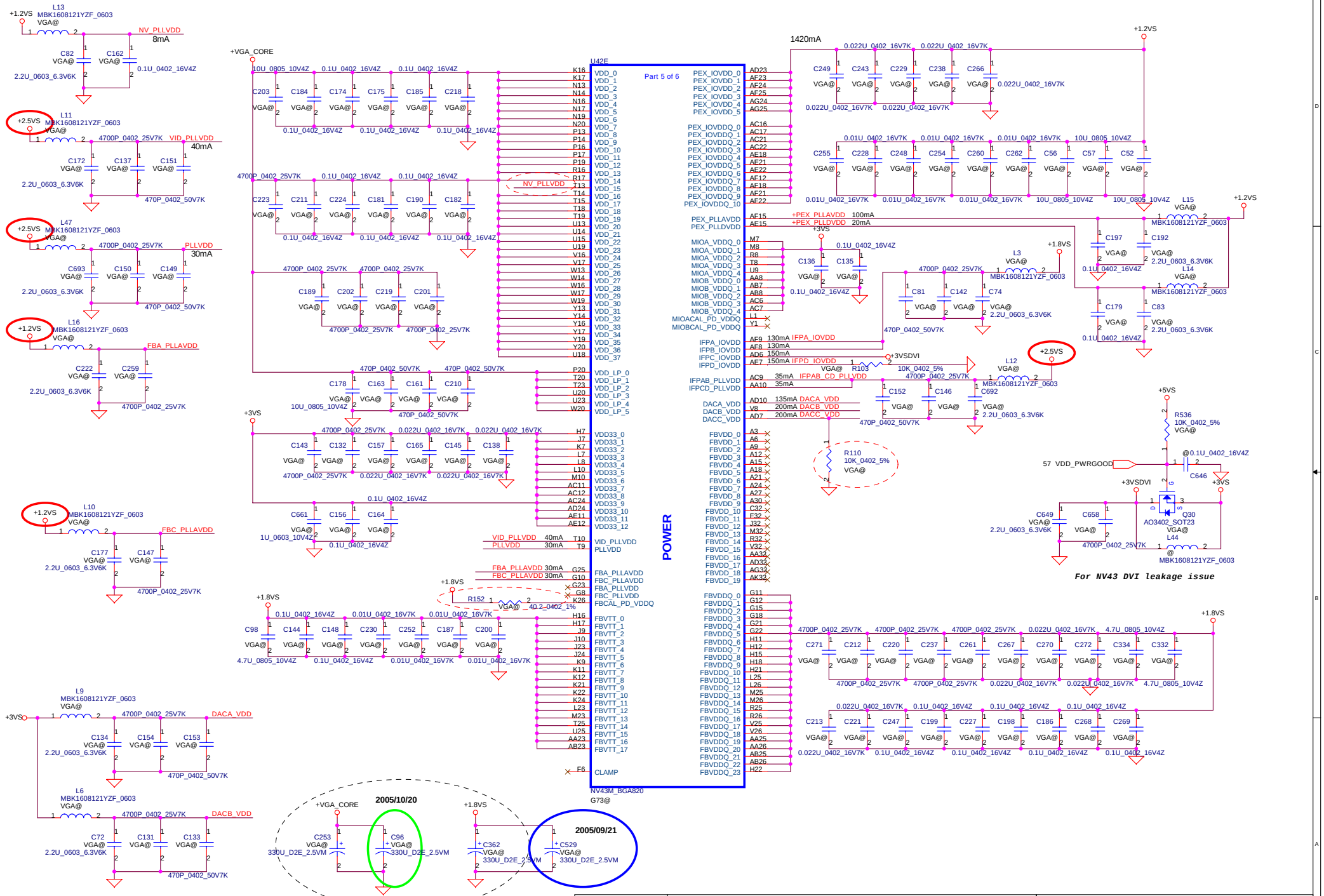

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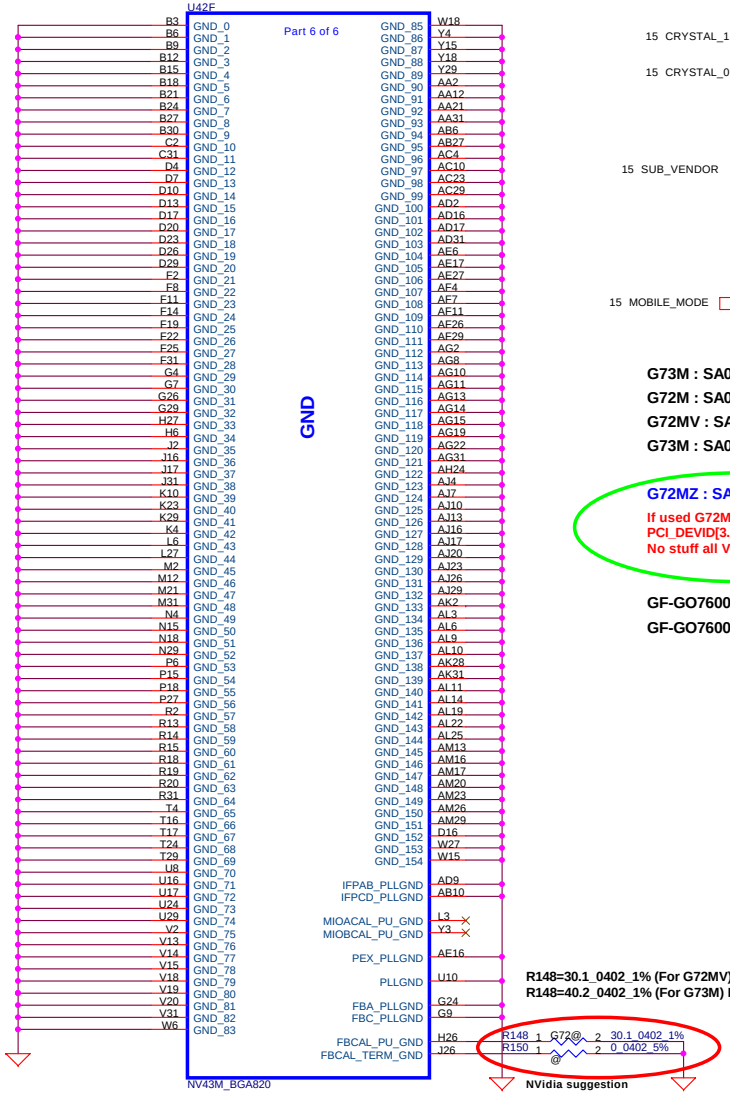
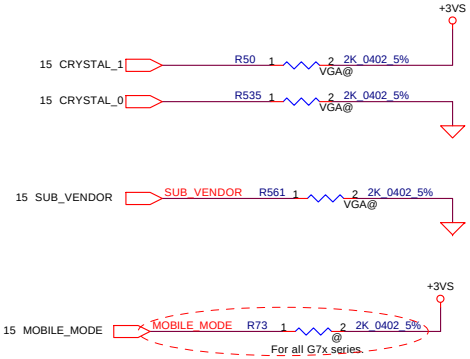




G73M : SA00000QZ00 (A1)

G72M : SA00000QY00

G72MV : SA00000QY20

G73M : SA00000QZ10 (A2)

G72MZ : SA00001BL00

If used G72MZ RAM_CFG[0..3]=0000
PCI_DEVID[3.2.1.0]=0110
No stuff all VRAM.

GF-GO7600-SE-N-B1 : SA00000QZ30

GF-GO7600SEHN-B1/H : SA00000QZ40

R148=30.1_0402_1% (For G72MV) P/N:SD00000B400
R148=40.2_0402_1% (For G73M) P/N:SD034402A80

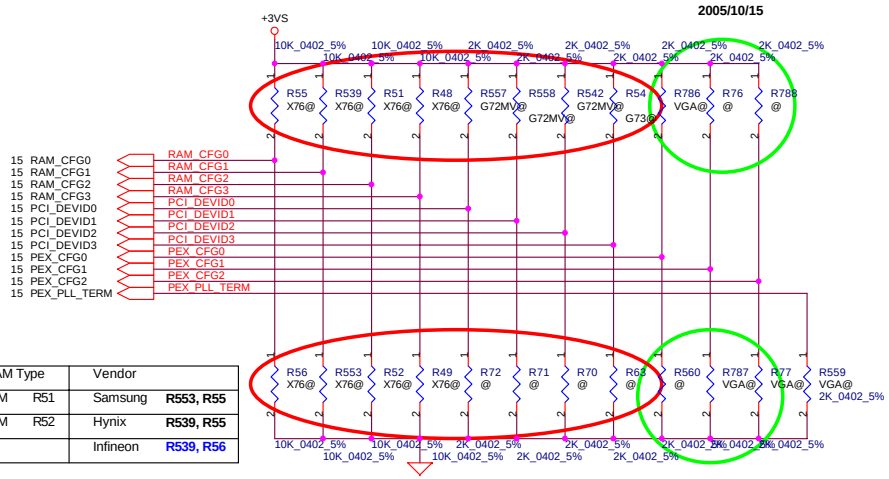
STRAPS	PIN	DESCRIPTION	G73M Value	G72MV Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	**RAM_CFG[3] (Bandwidth 0=Full, 1=Half)**		
		RAM_CFG[2] (0=16M or 1=32M)		
		RAM_CFG[1:0] (Manufacture) (01=Sam, 10=Inf, 11=Hyn)		
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

RAM_CFG[1:0]
(Manufacture)
(01=Sam, 10=Inf, 11=Hyn)

RAM_CFG[2] (0=16M or 1=32M)

RAM_CFG[3] (Bandwidth 0=Full, 1=Half)

2005/10/15



Bandwidth		RAM Type		Vendor	
FULL	R49	32M	R51	Samsung	**R553, R55**
HALF	R48	16M	R52	Hynix	**R539, R55**
				Infineon	**R539, R56**

Package		
(10*12.5)	**Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)**	**Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)**
(11*13)	**Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)**	**Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)**
(8*13)	**Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)**	**Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)**

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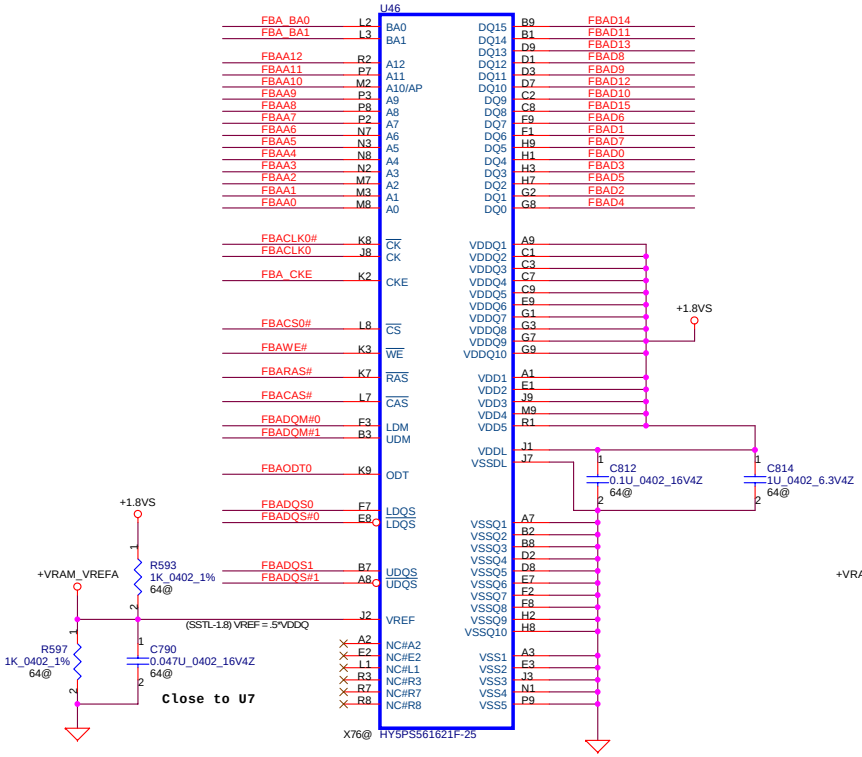
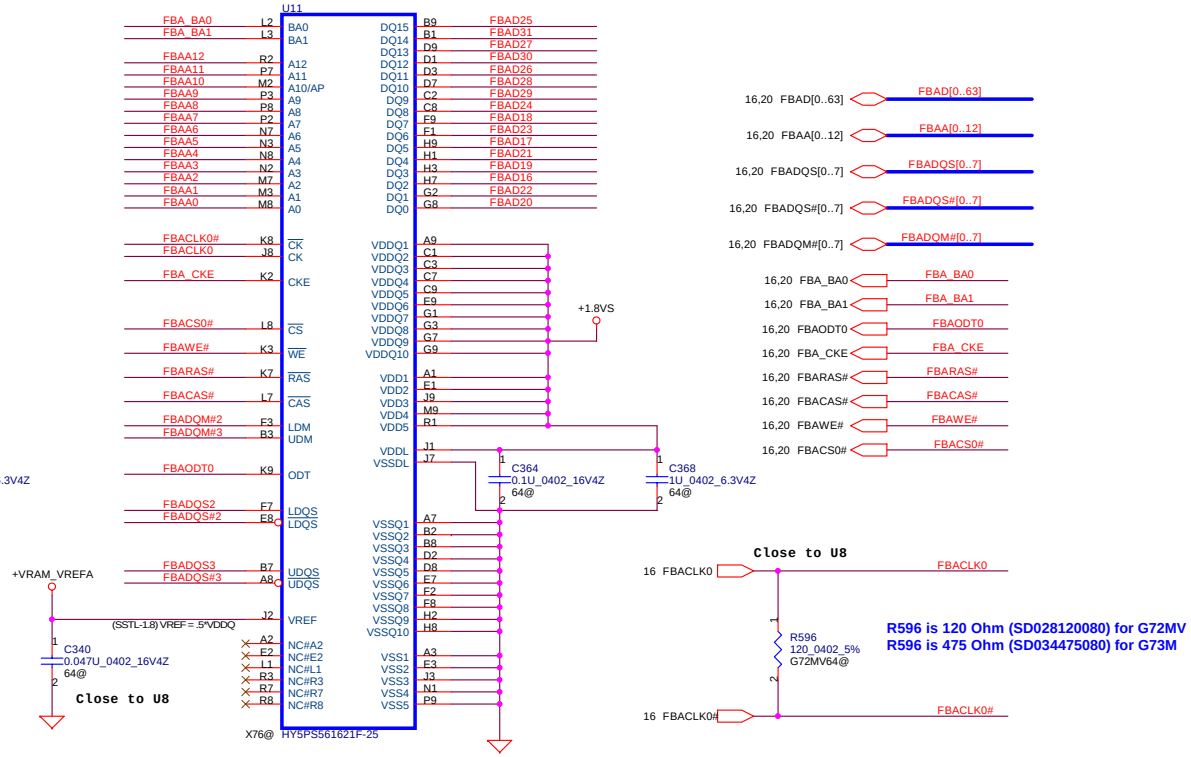
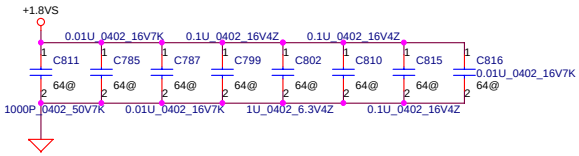
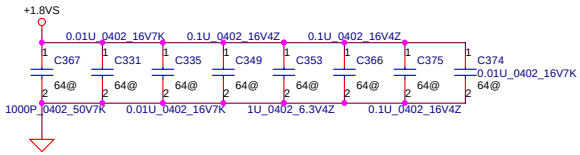


DDR2 BGA MEMORY



DDR2 BGA MEMORY





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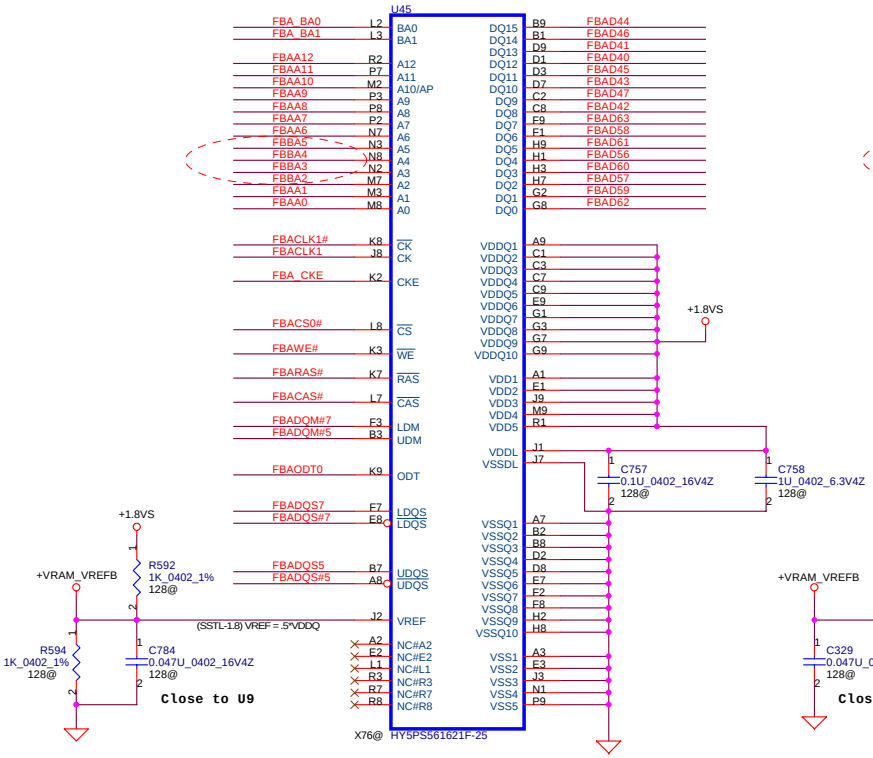

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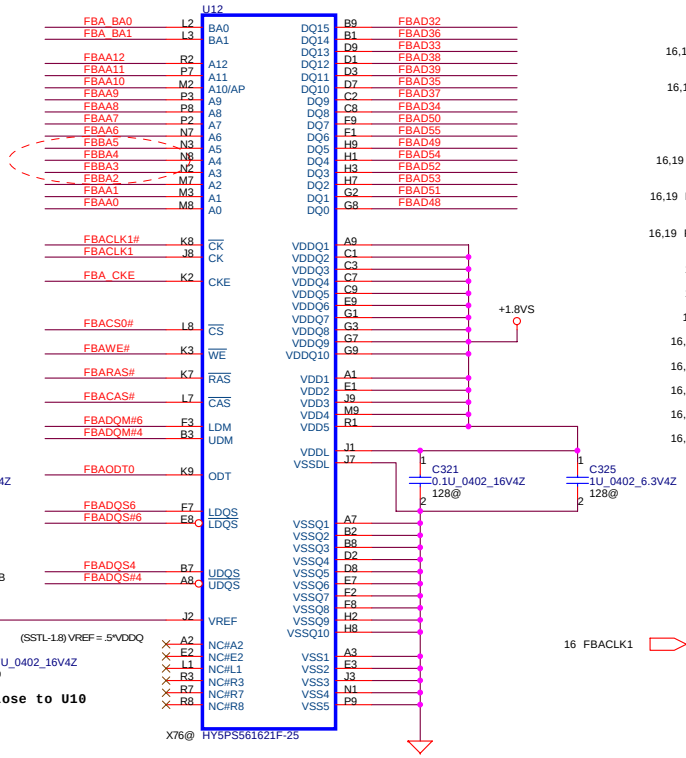

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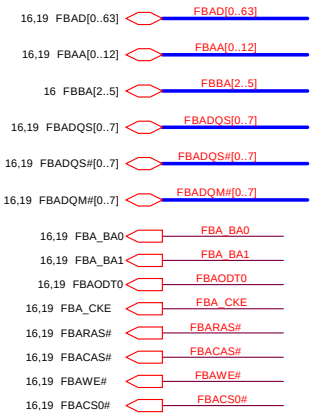
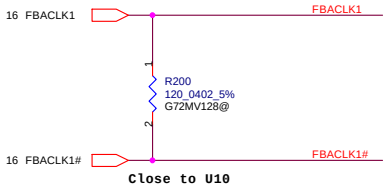
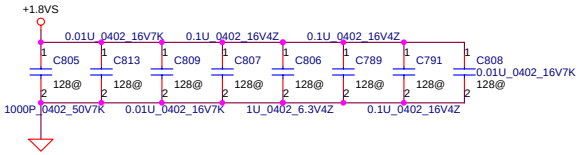
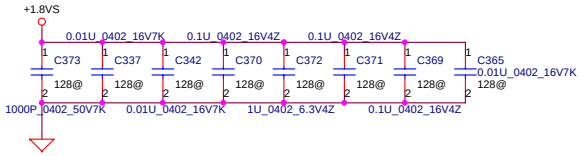




R200 is 120 Ohm (SD028120080) for G72MV
R200 is 475 Ohm (SD034475080) for G73M





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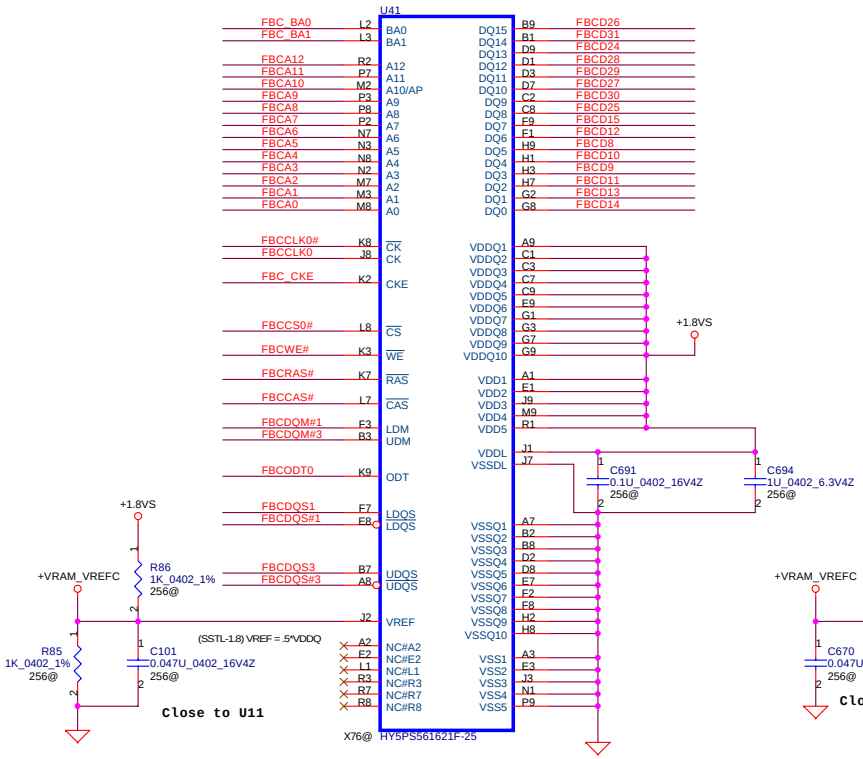

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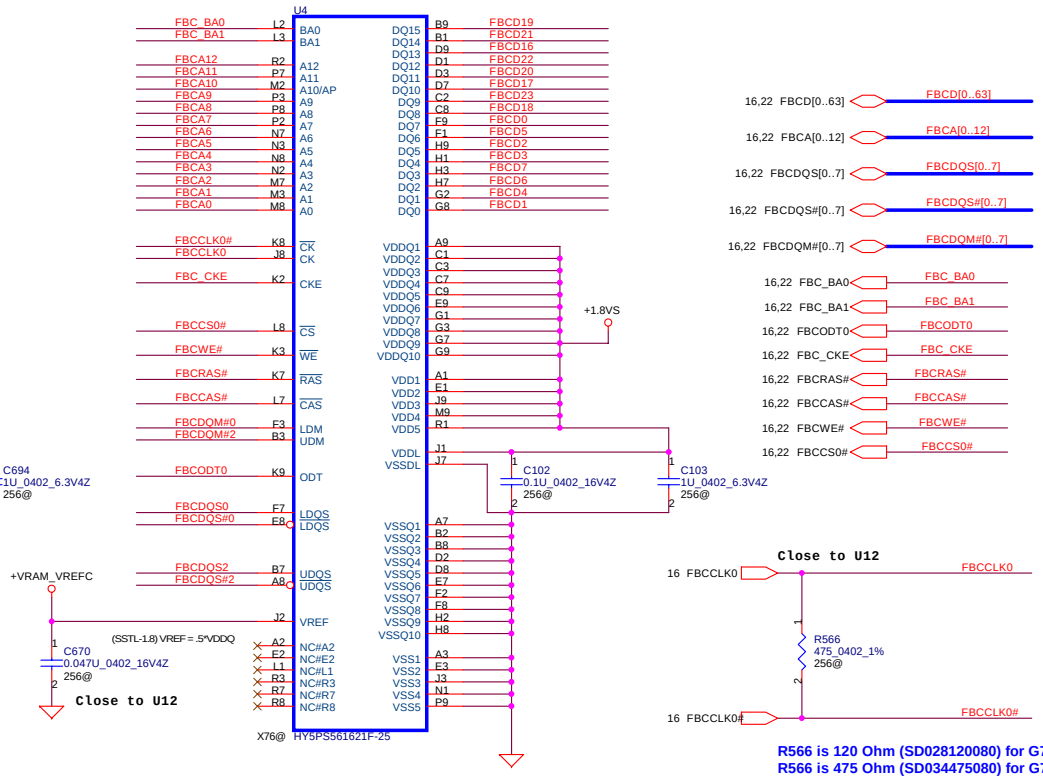

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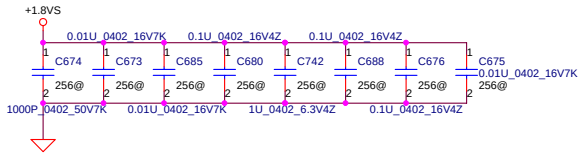

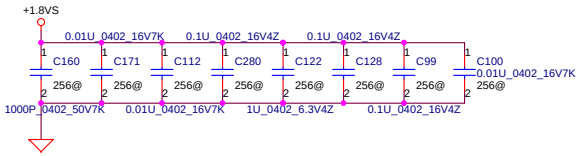

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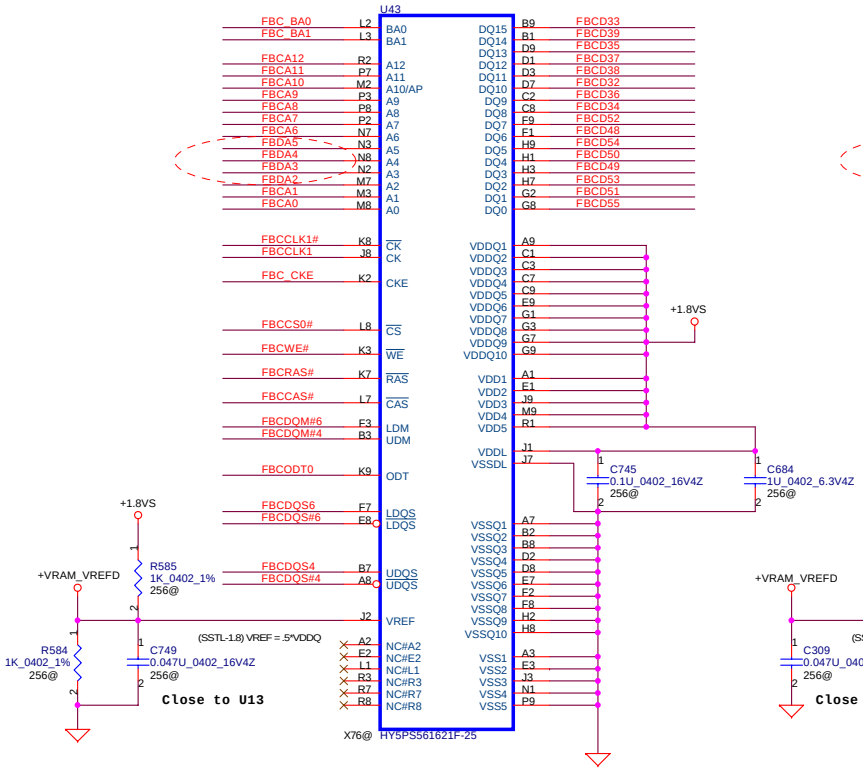

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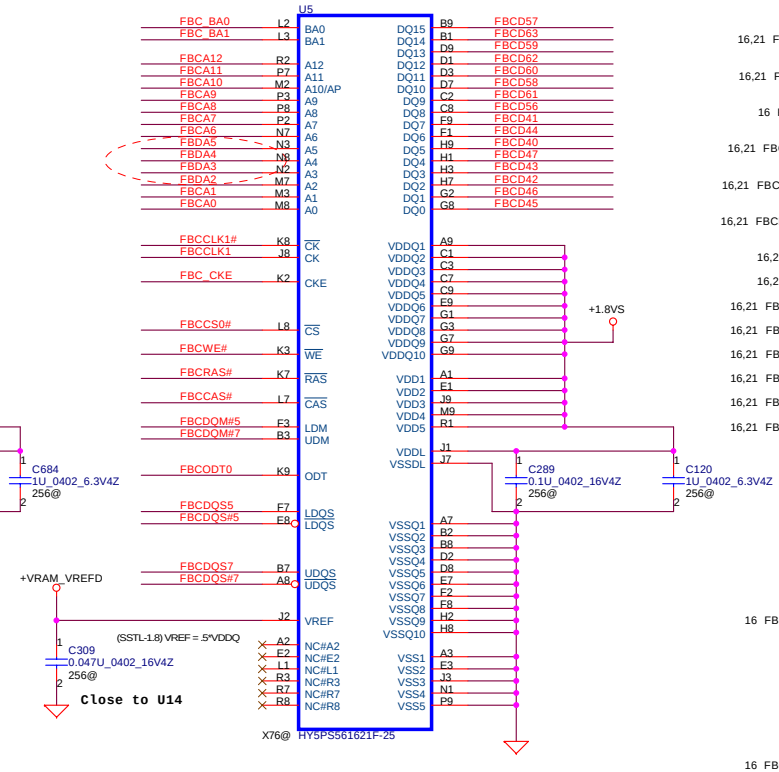

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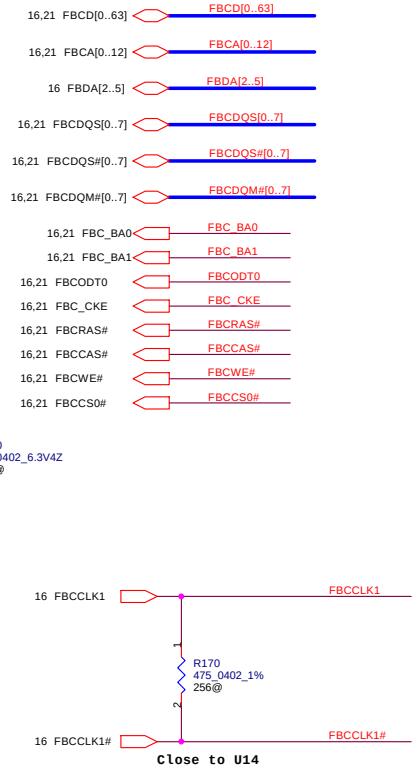
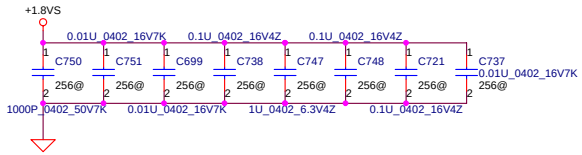
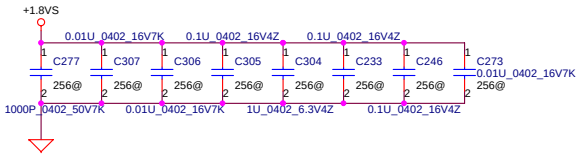


R170 is 120 Ohm (SD028120080) for G72MV
R170 is 475 Ohm (SD034475080) for G73M





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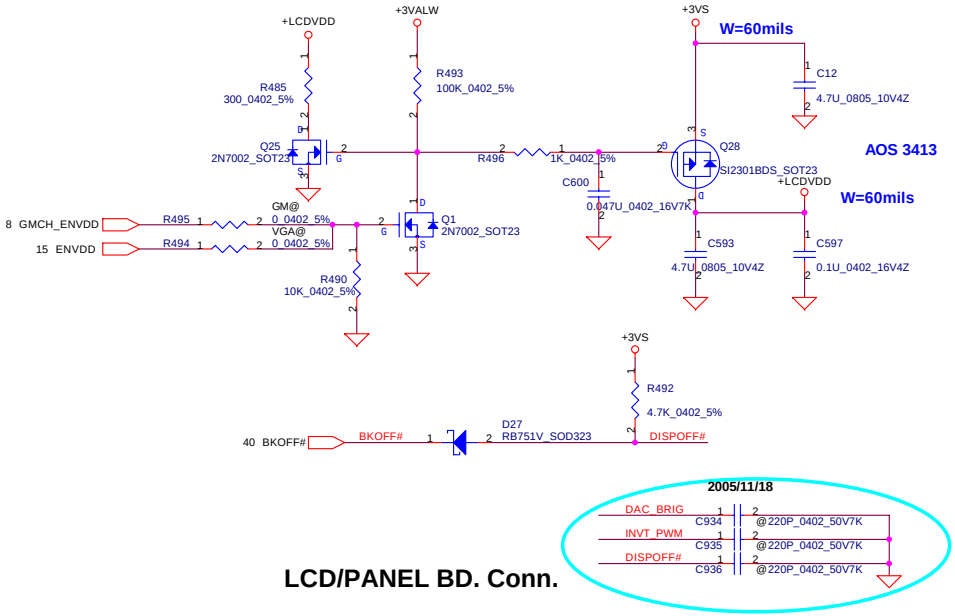
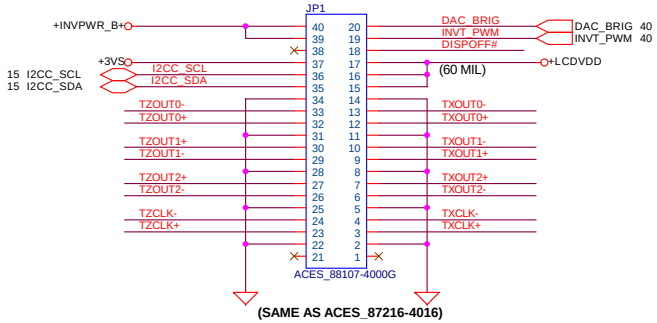
LCD POWER CIRCUIT



2005/11/18

LCD/PANEL BD. Conn.



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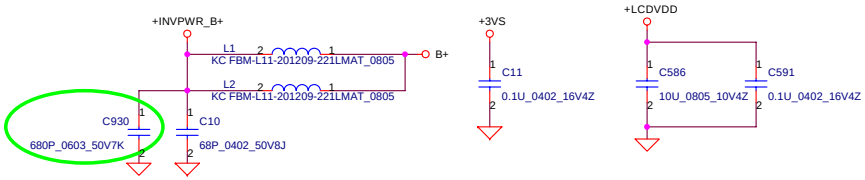

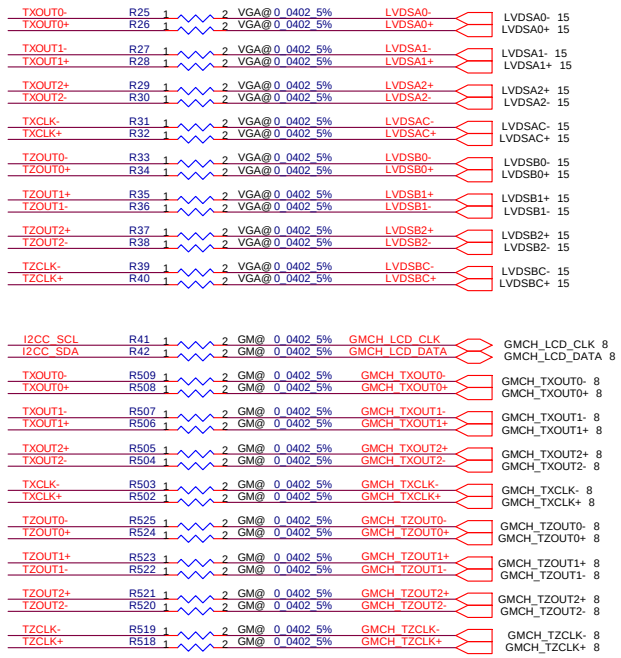

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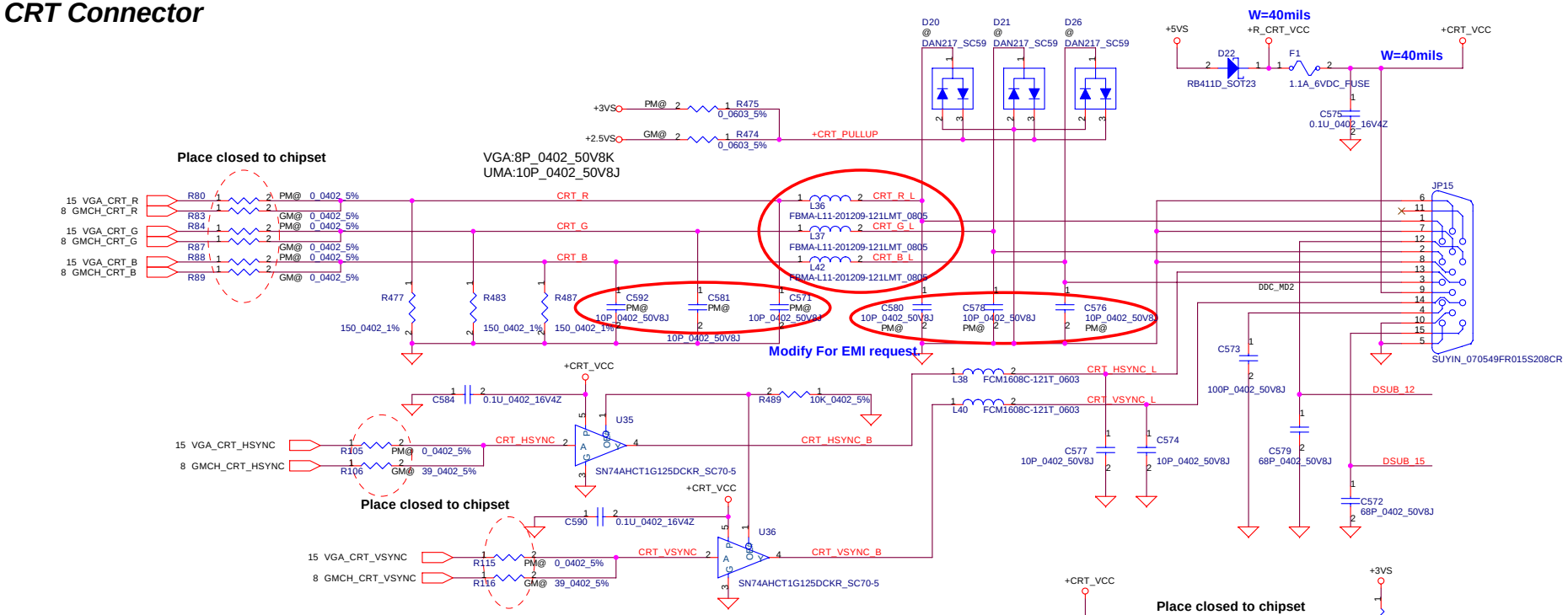
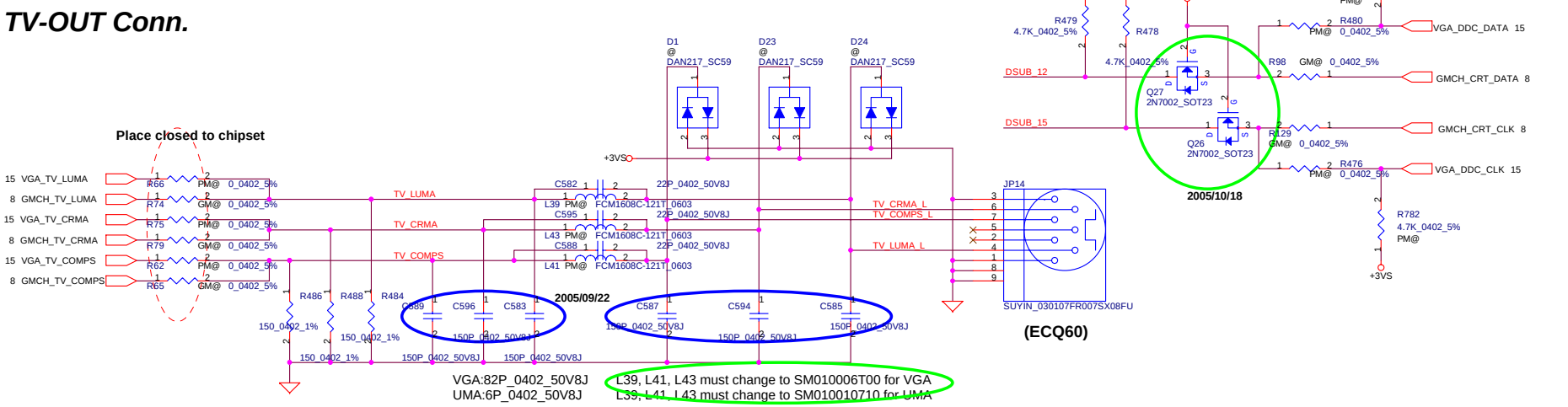
CRT Connector



TV-OUT Conn.



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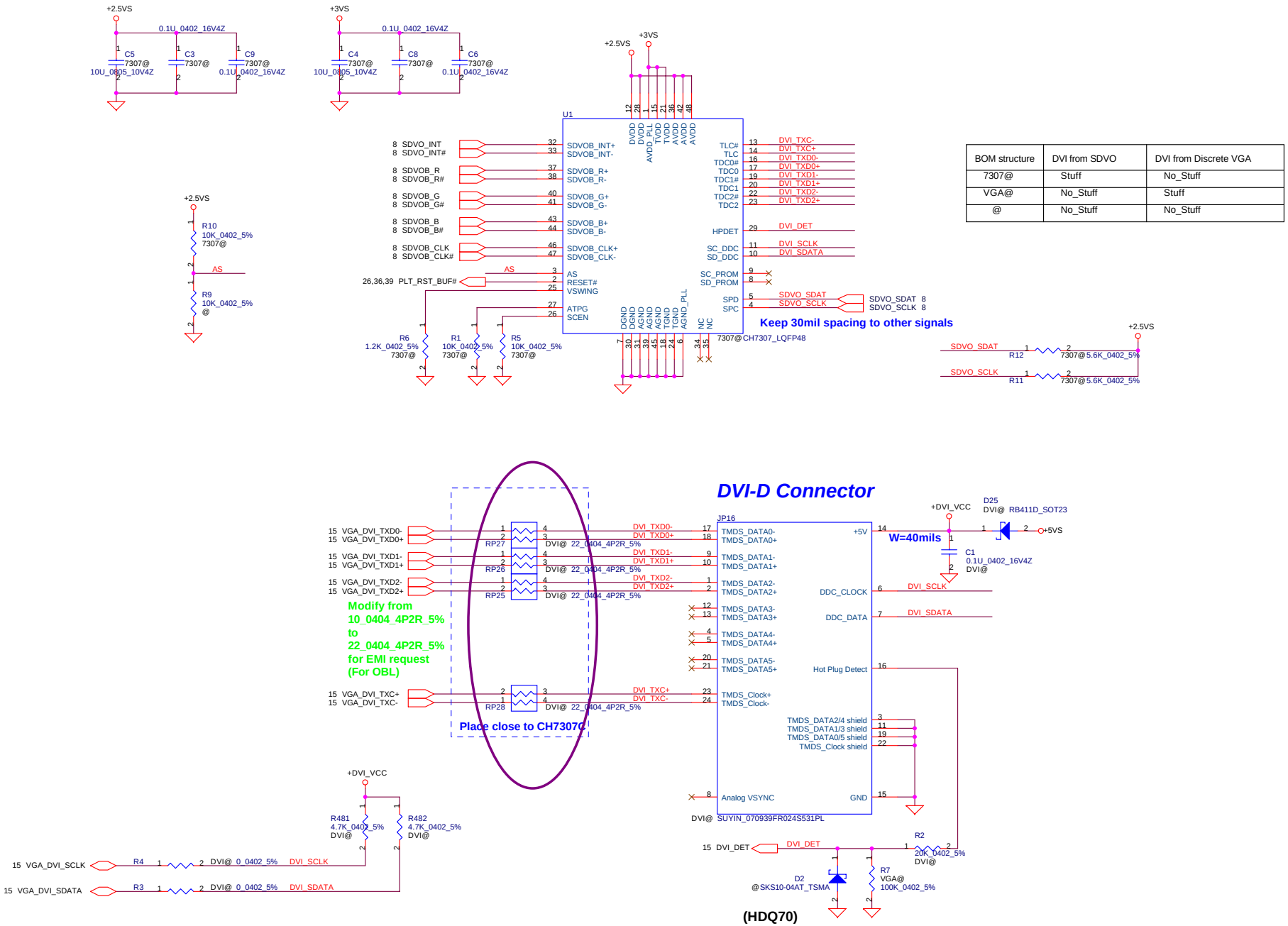

BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

Security Classification	Compal Secret Data		
Issued Date	2006/10/4	Deciphered Date	2007/10/4

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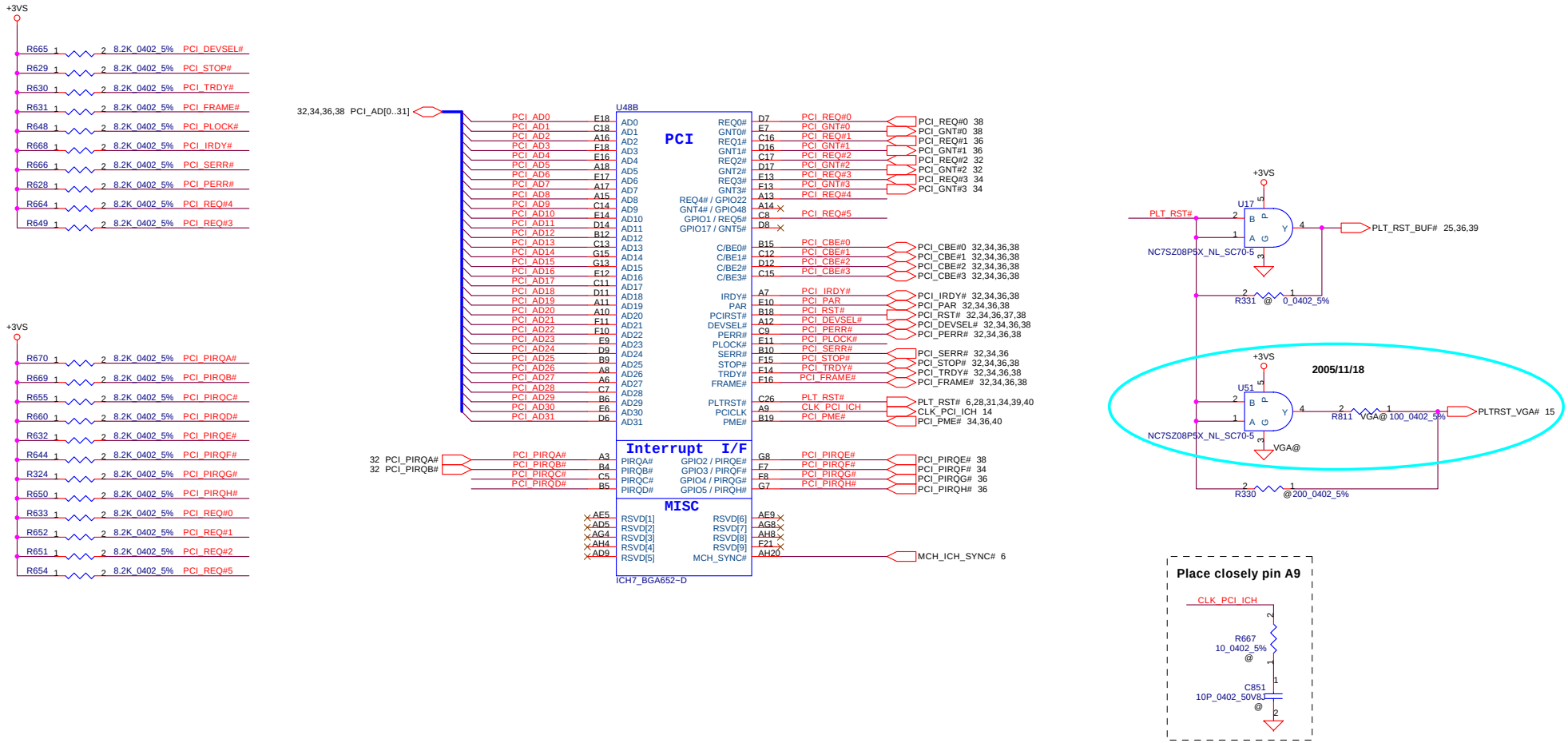
ICH7M(SL8YB)[B-0]:SA00000V190(ABO!)



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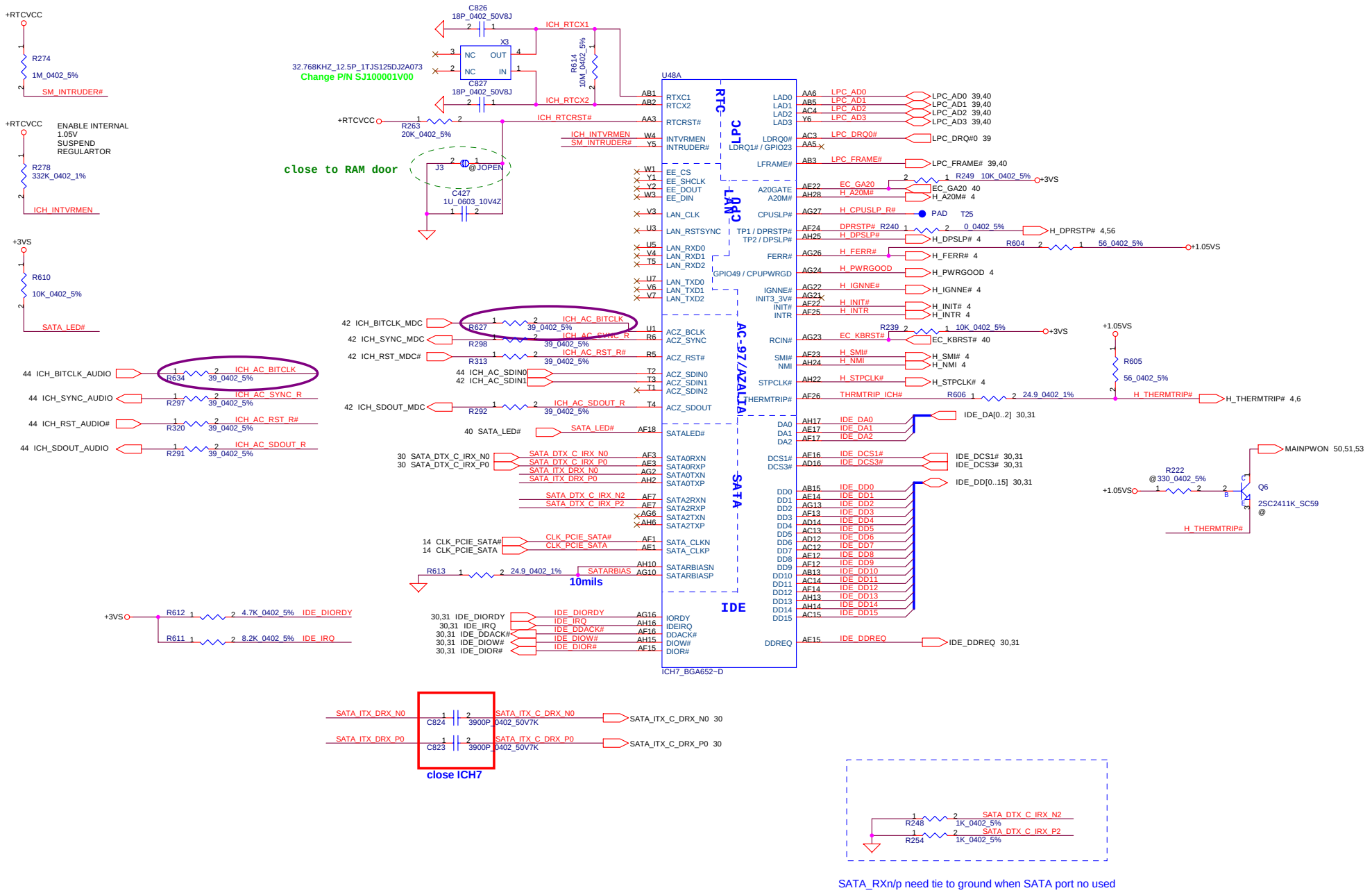

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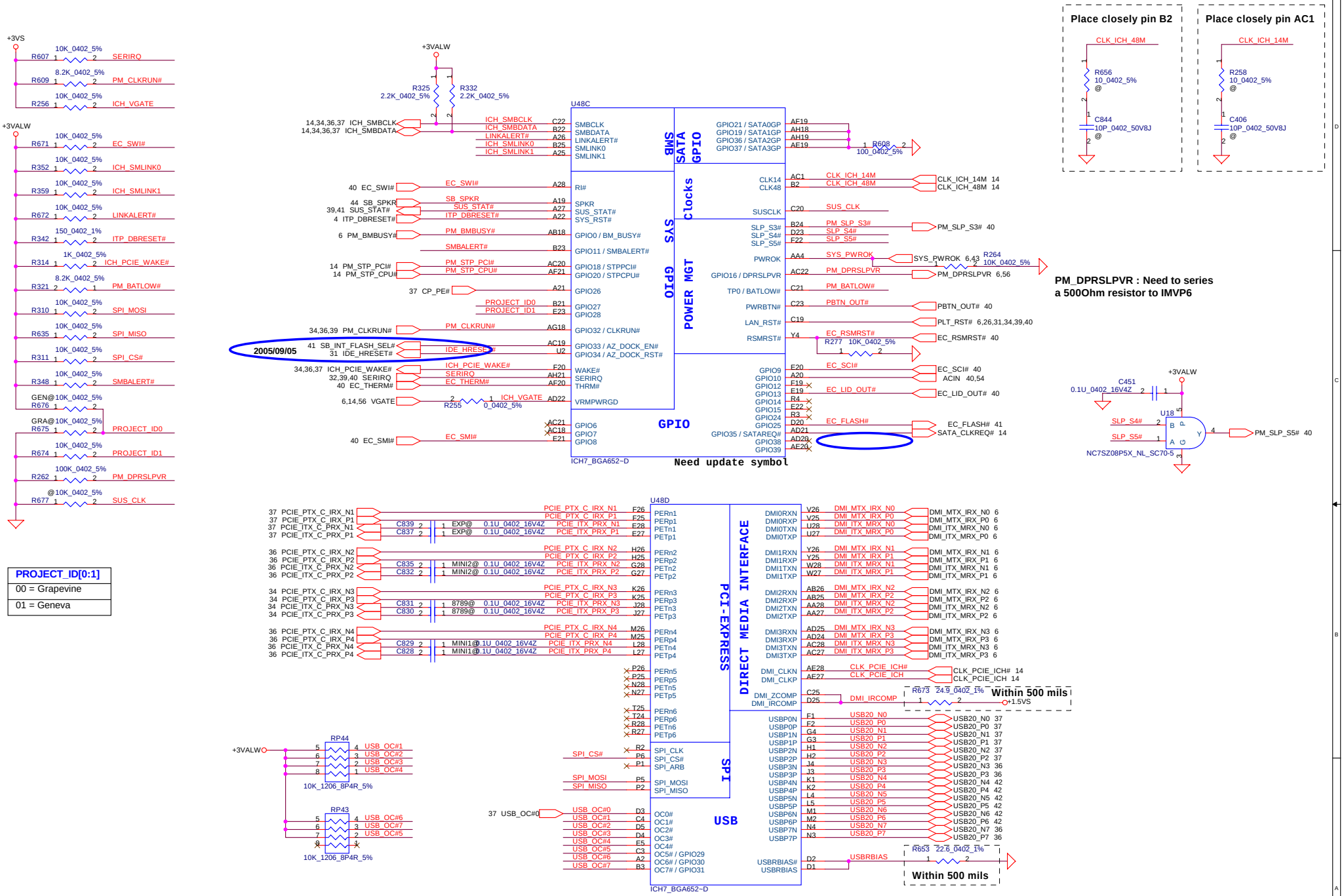

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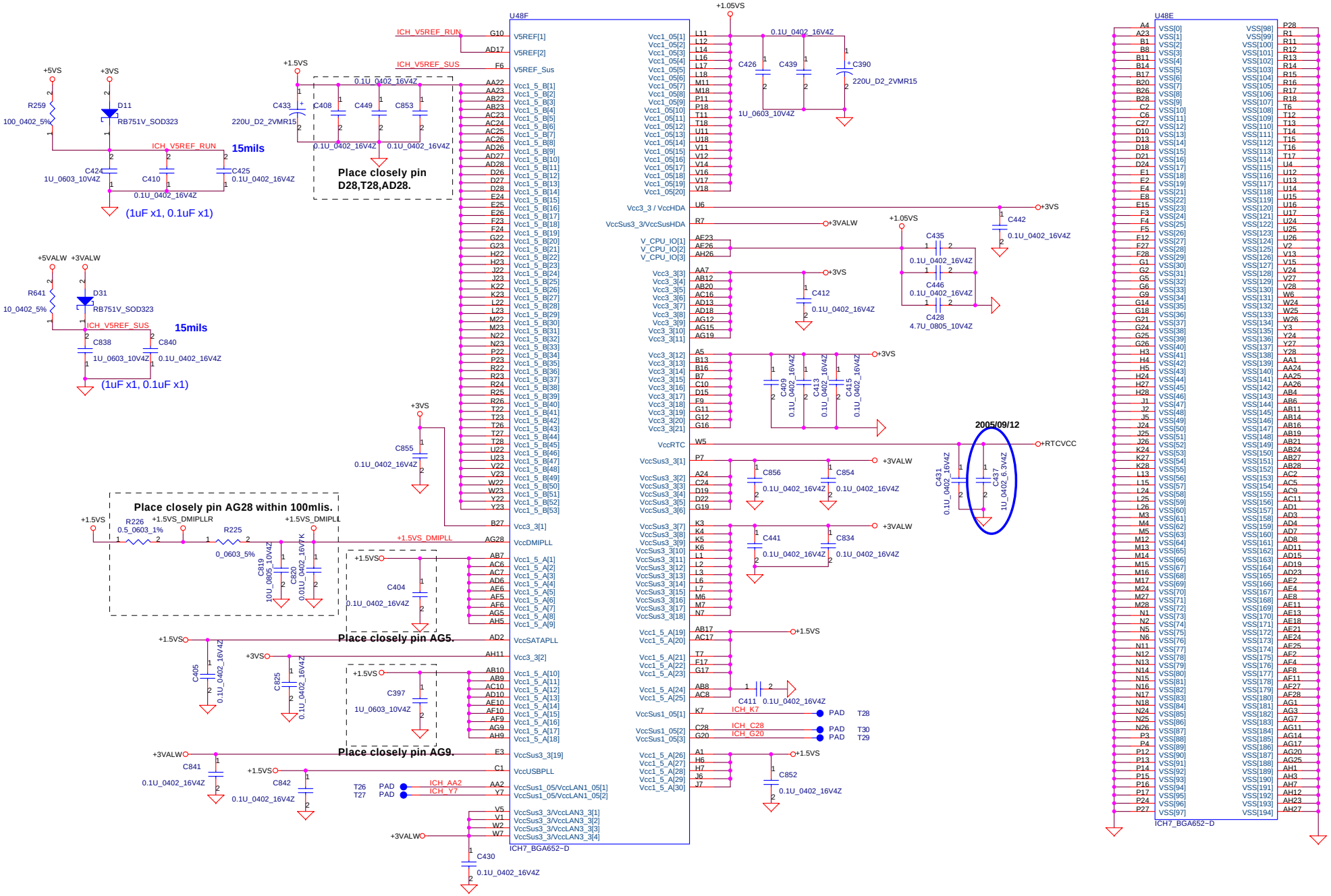

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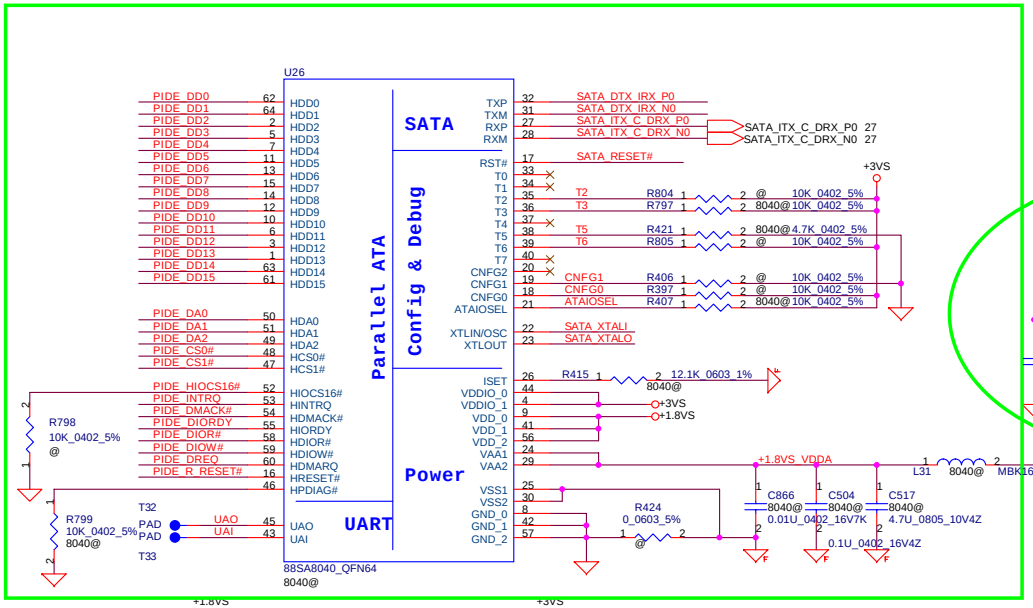

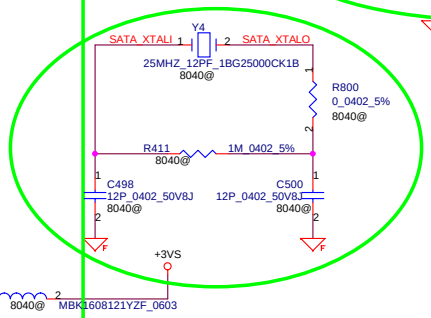

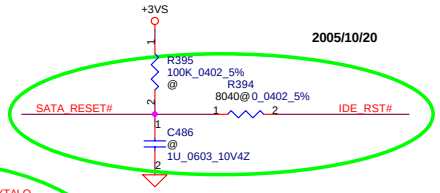

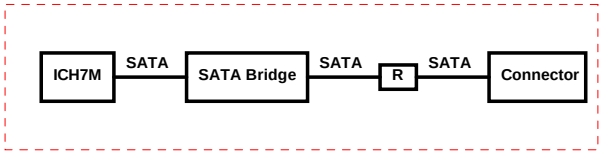

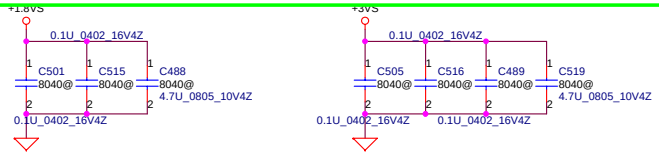

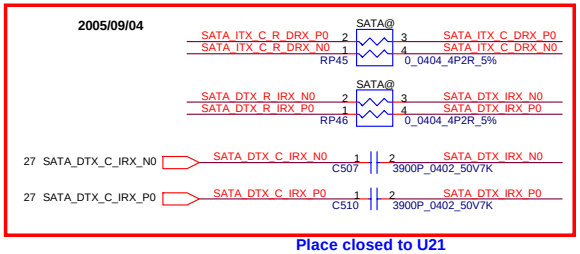

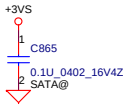

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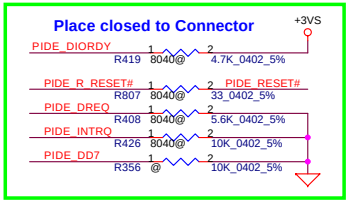

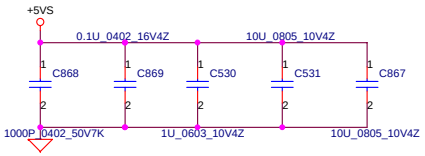

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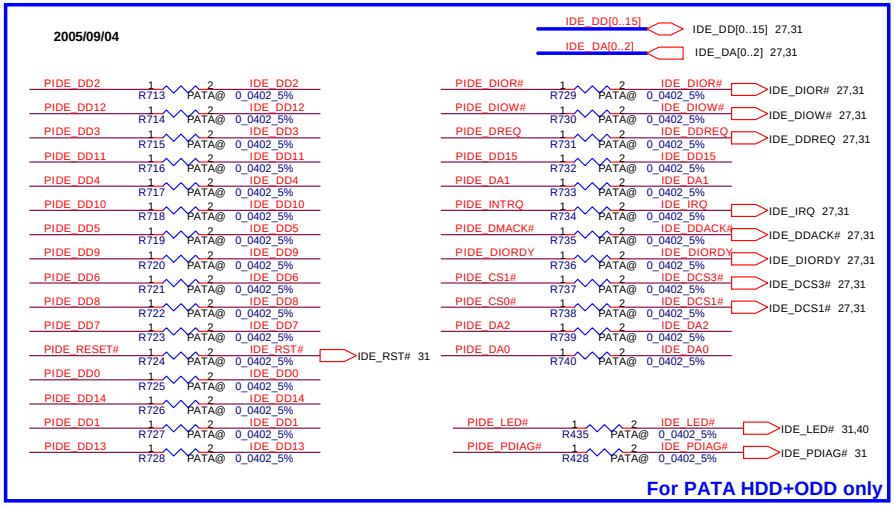

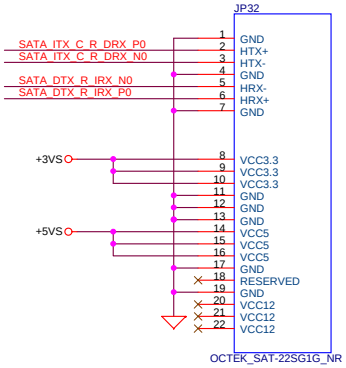

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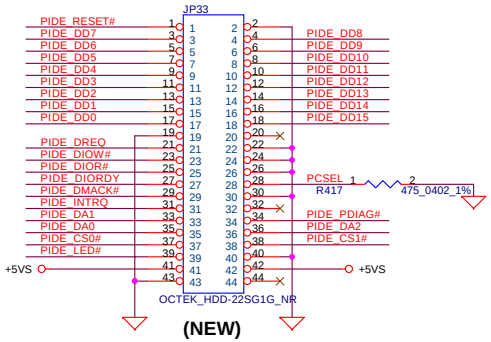
Change Library



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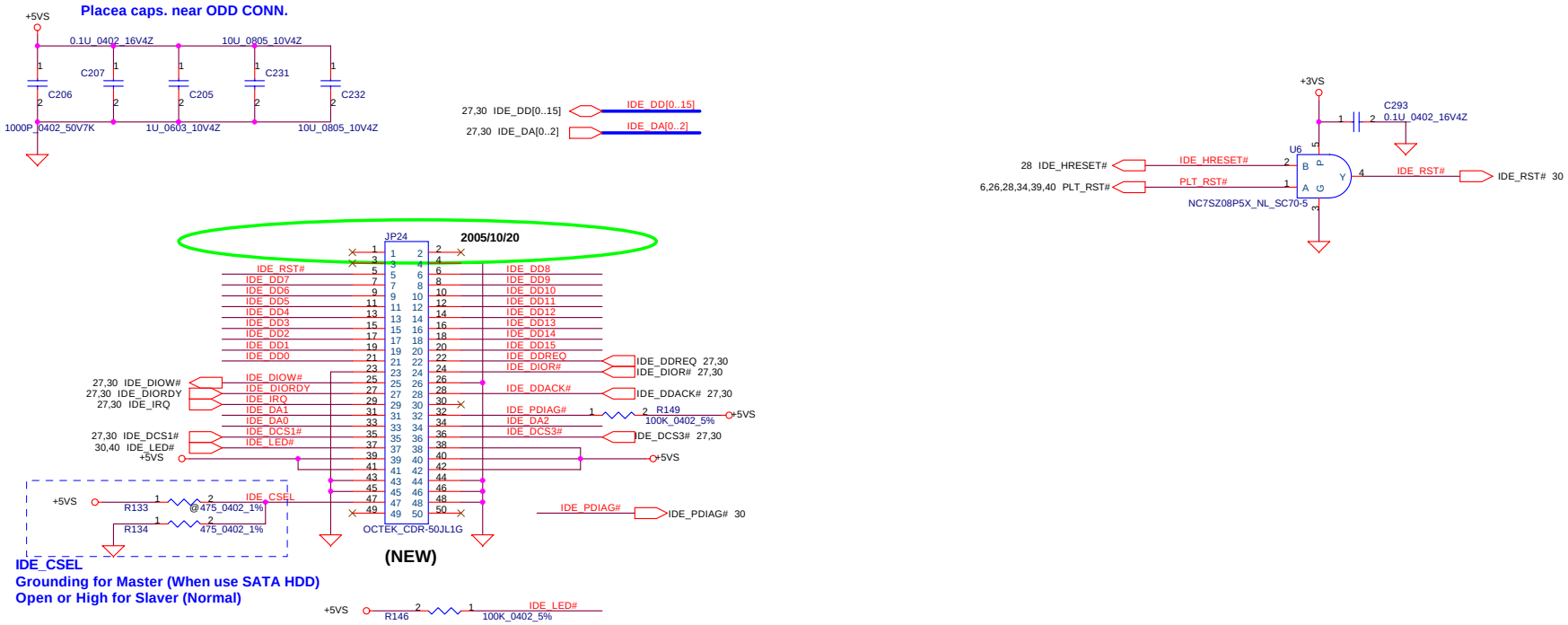

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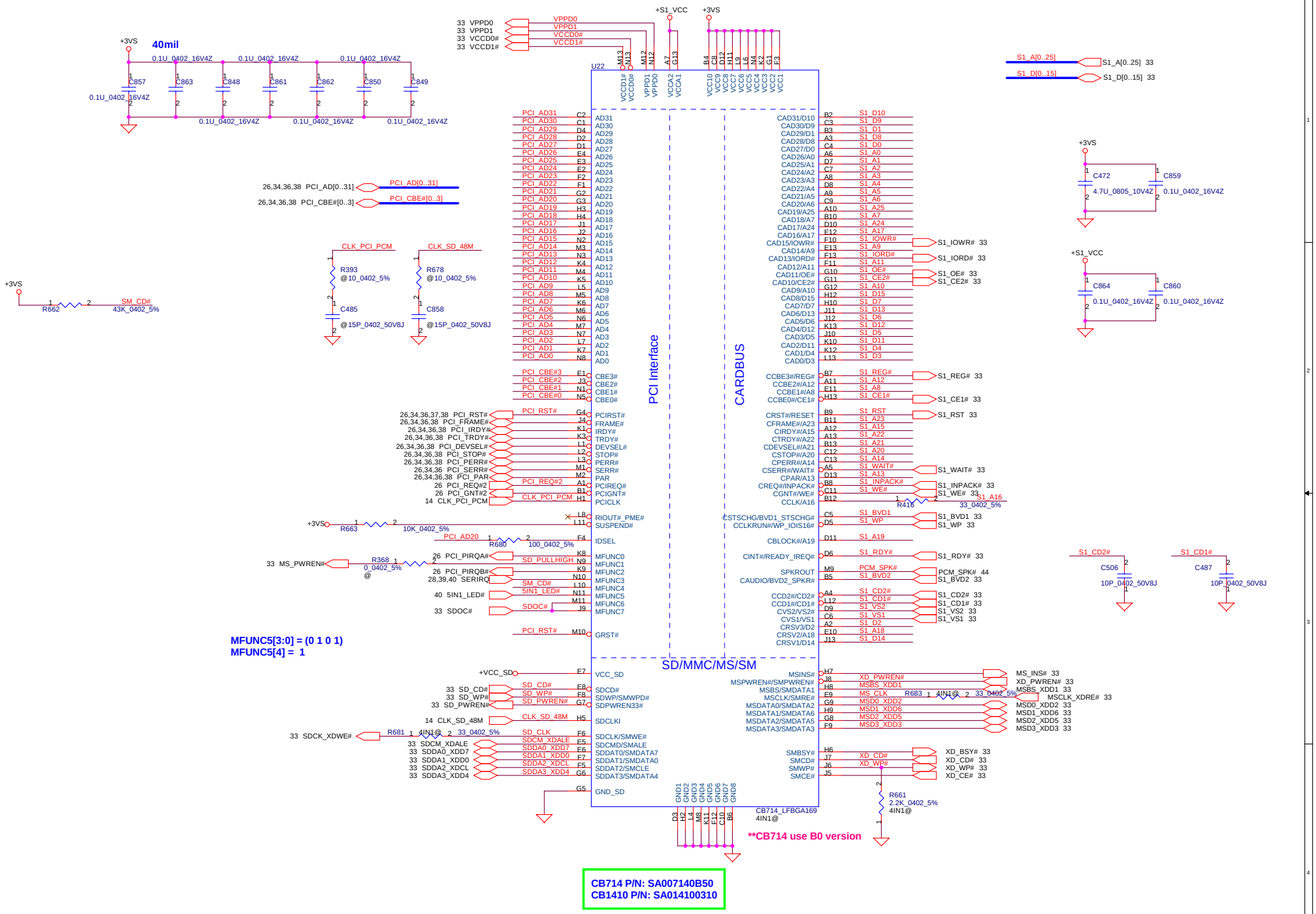

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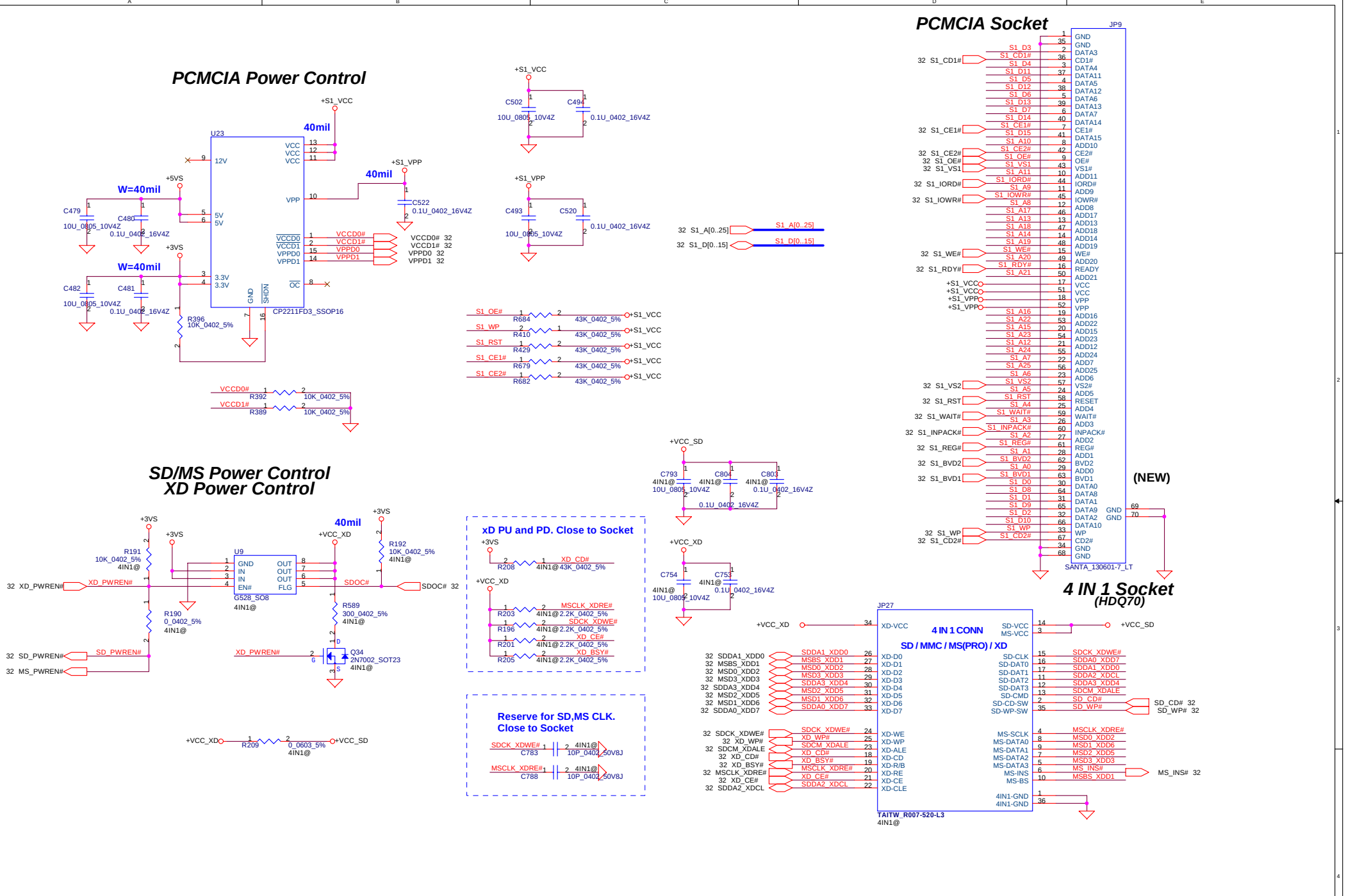

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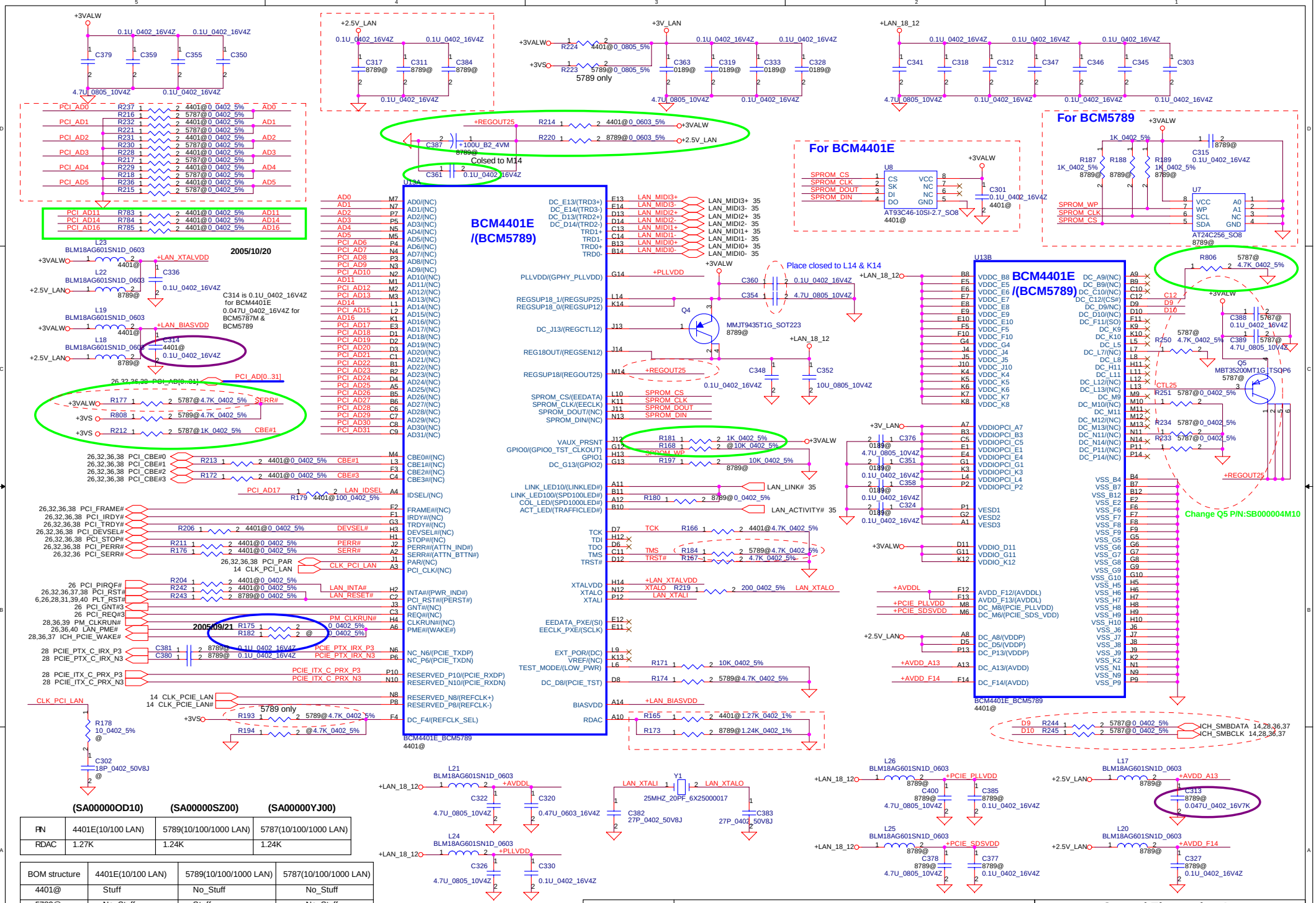

	(SA00000OD10)	(SA00000SZ00)	(SA00000YJ00)
PIN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

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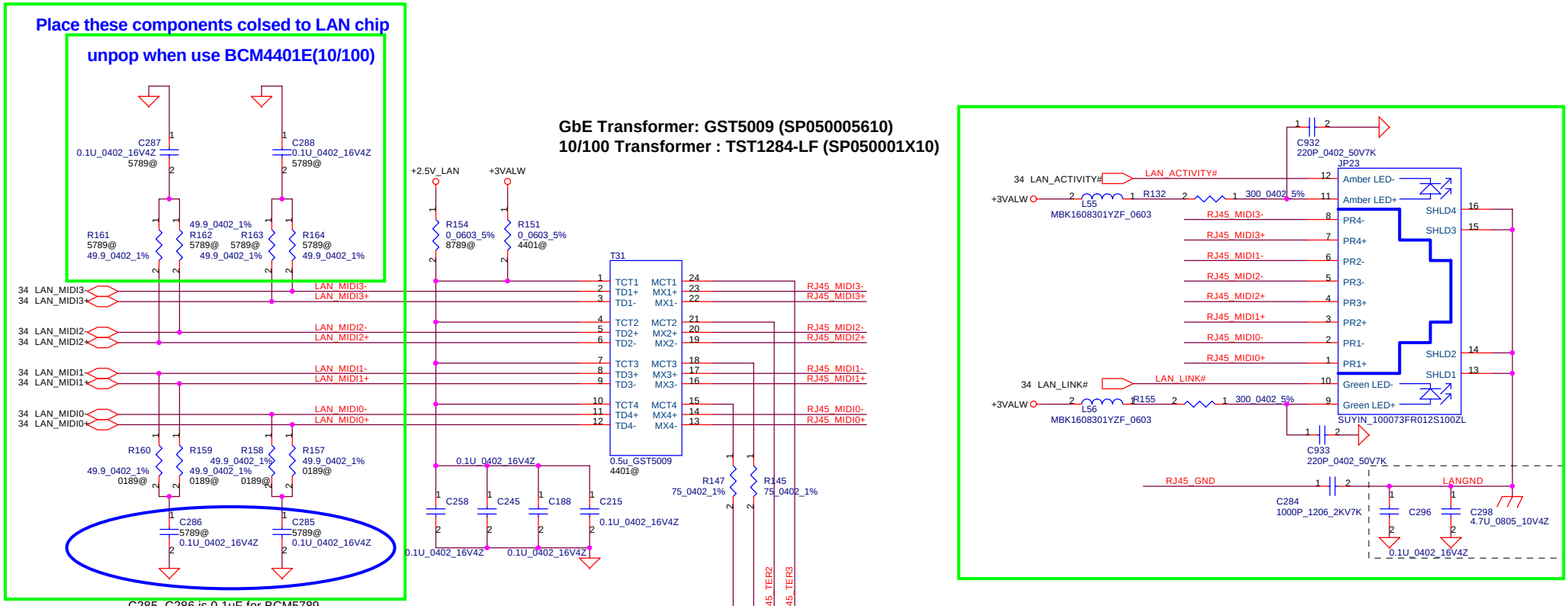
LAN BCM4401E/ BCM5789



C285, C286 is 0.1uF for BCM5789.
C285, C286 is 0.01uF for BCM4401E.

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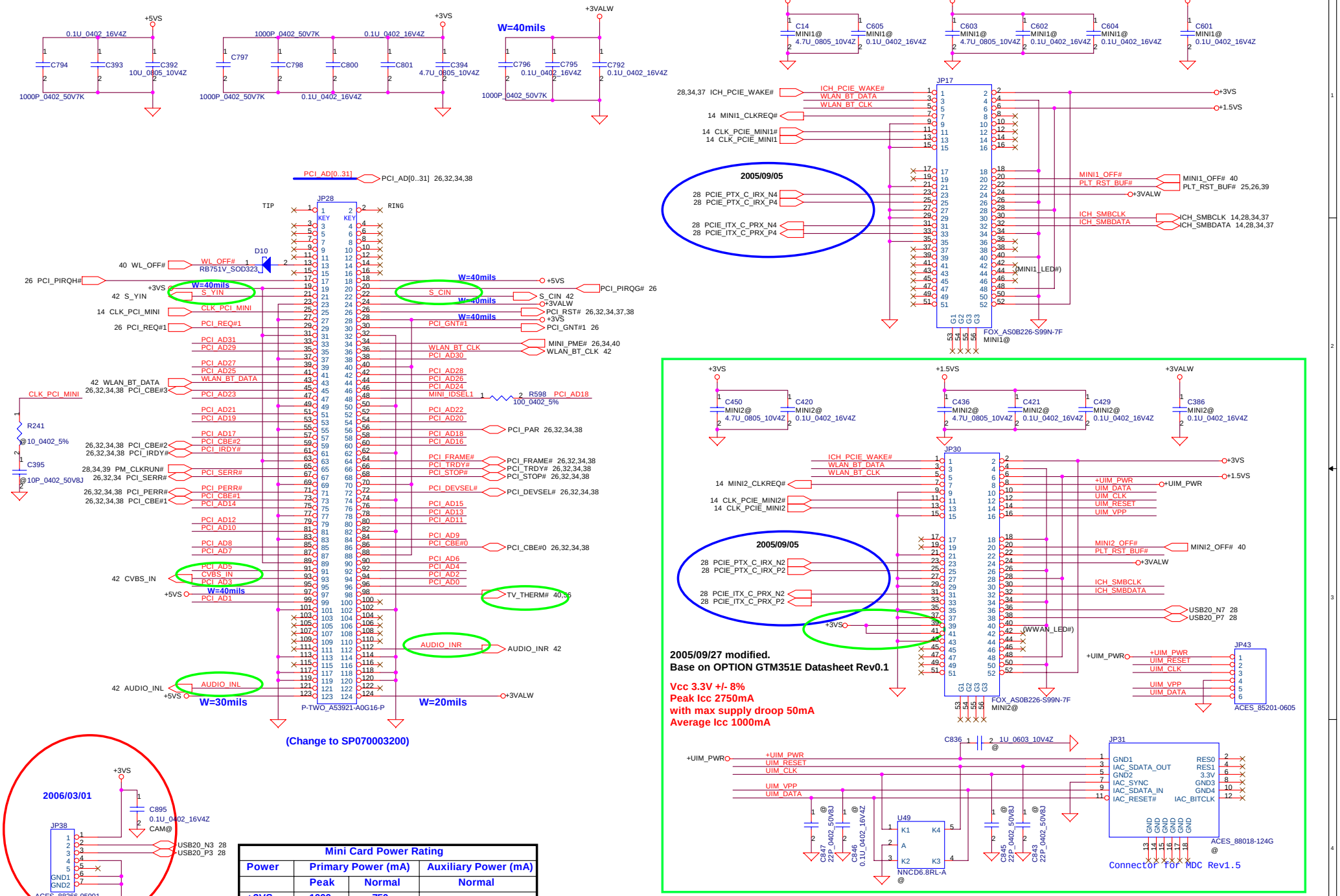

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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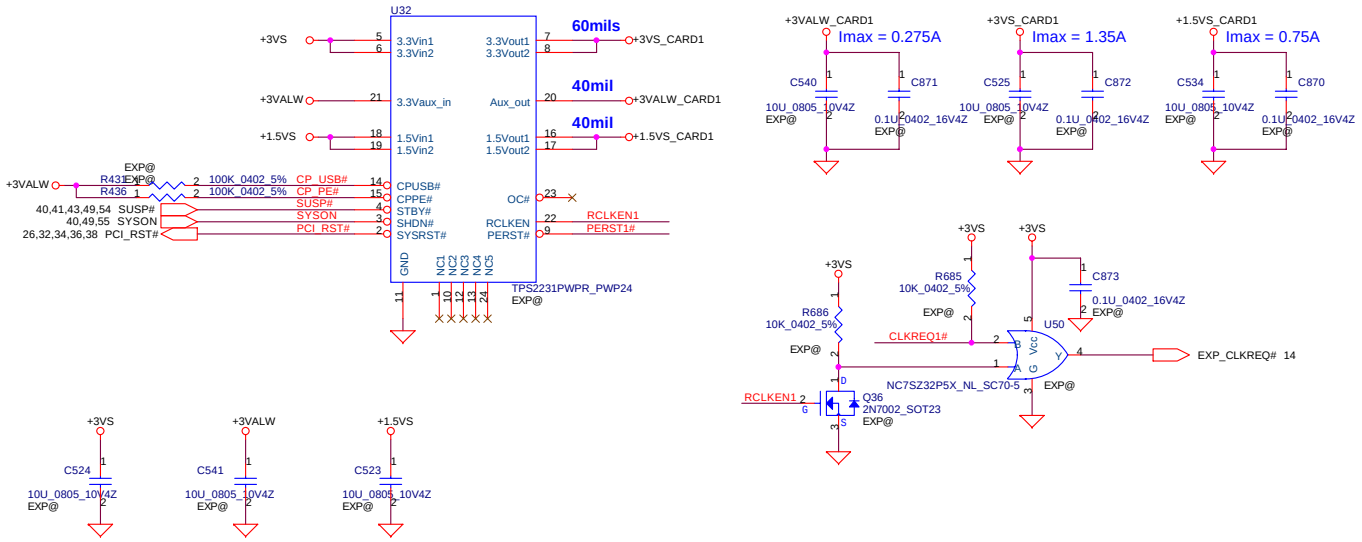
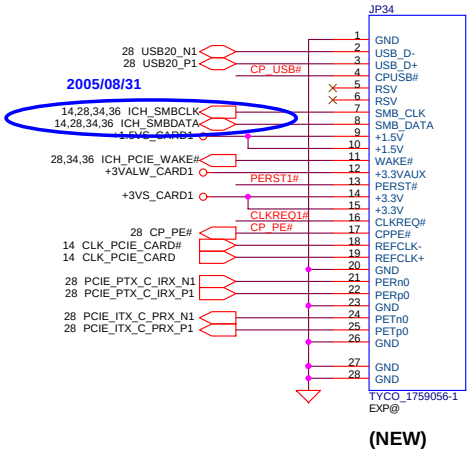
New Card Power Switch

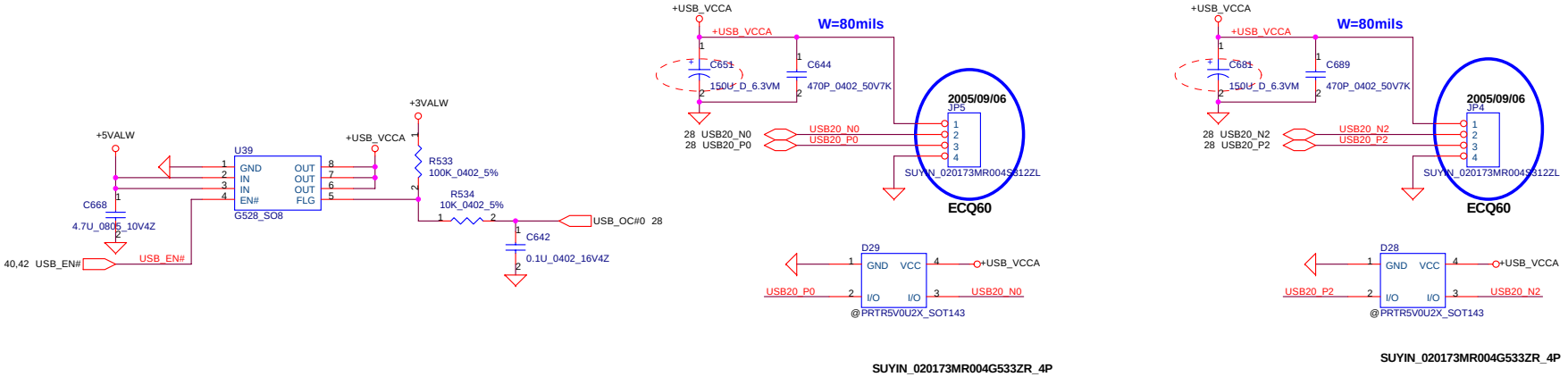


New Card Socket (Left)



(NEW)

USB CONN. 1 & 2



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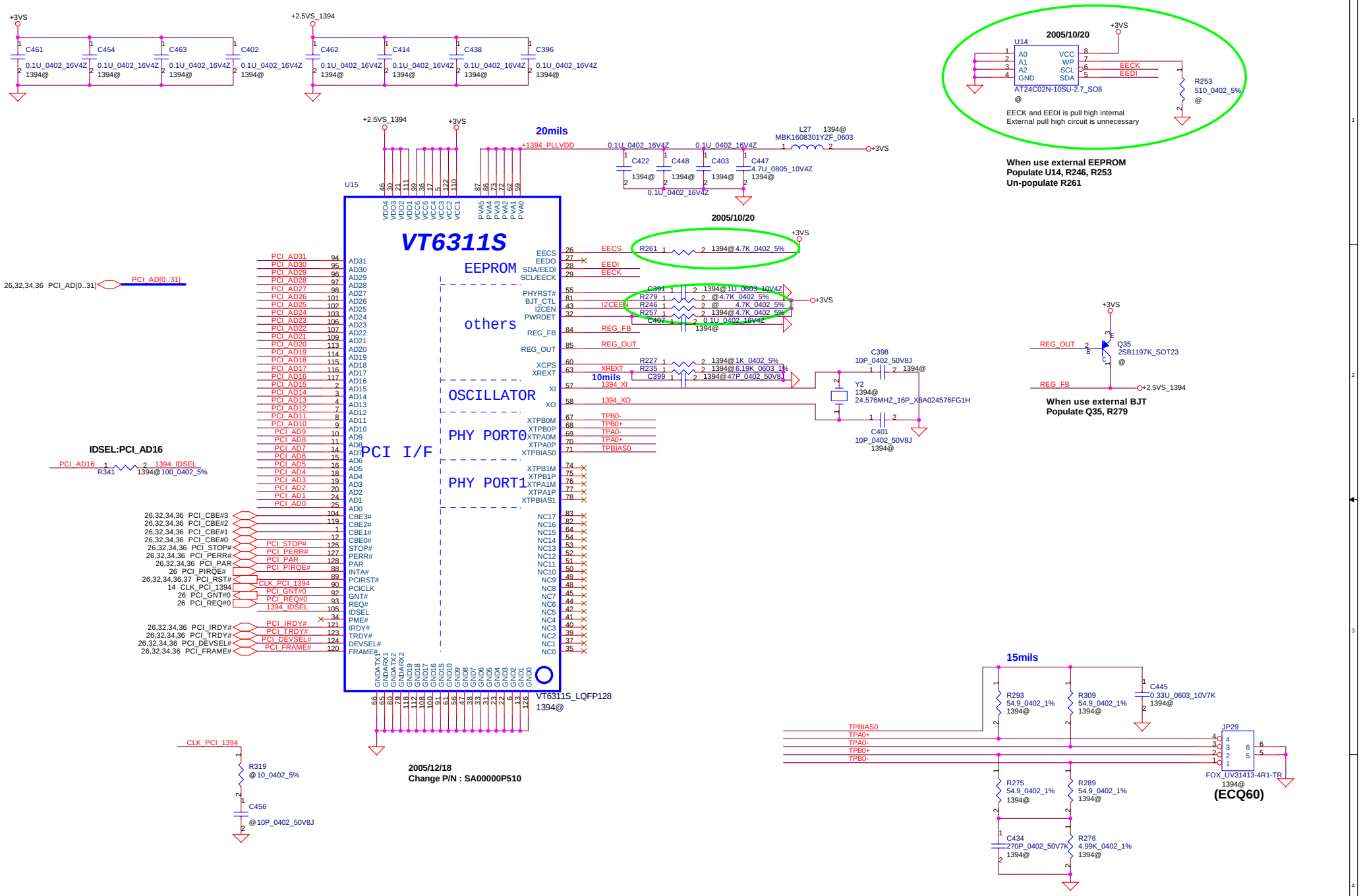

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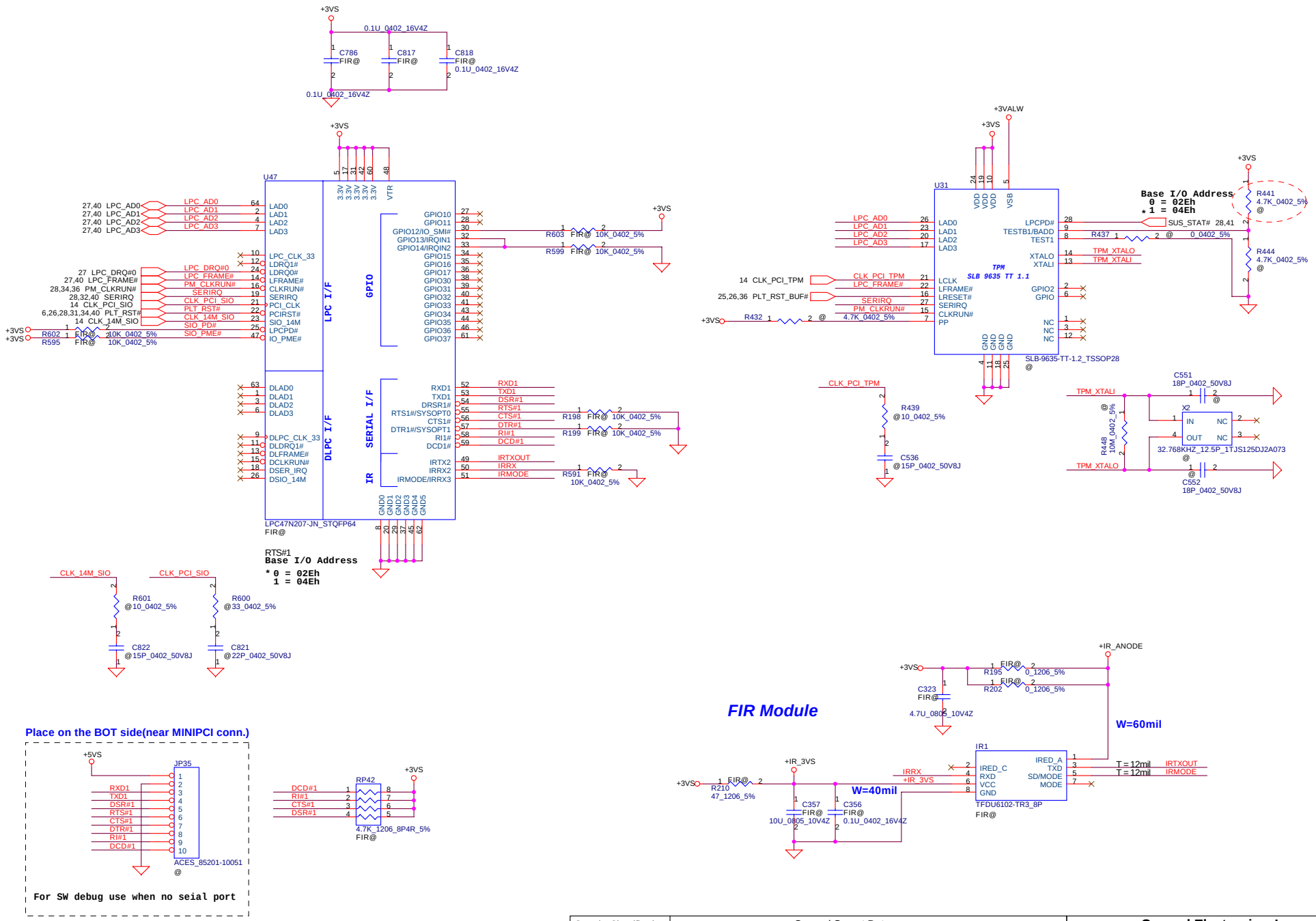
SUPER I/O SMsC LPC47N207



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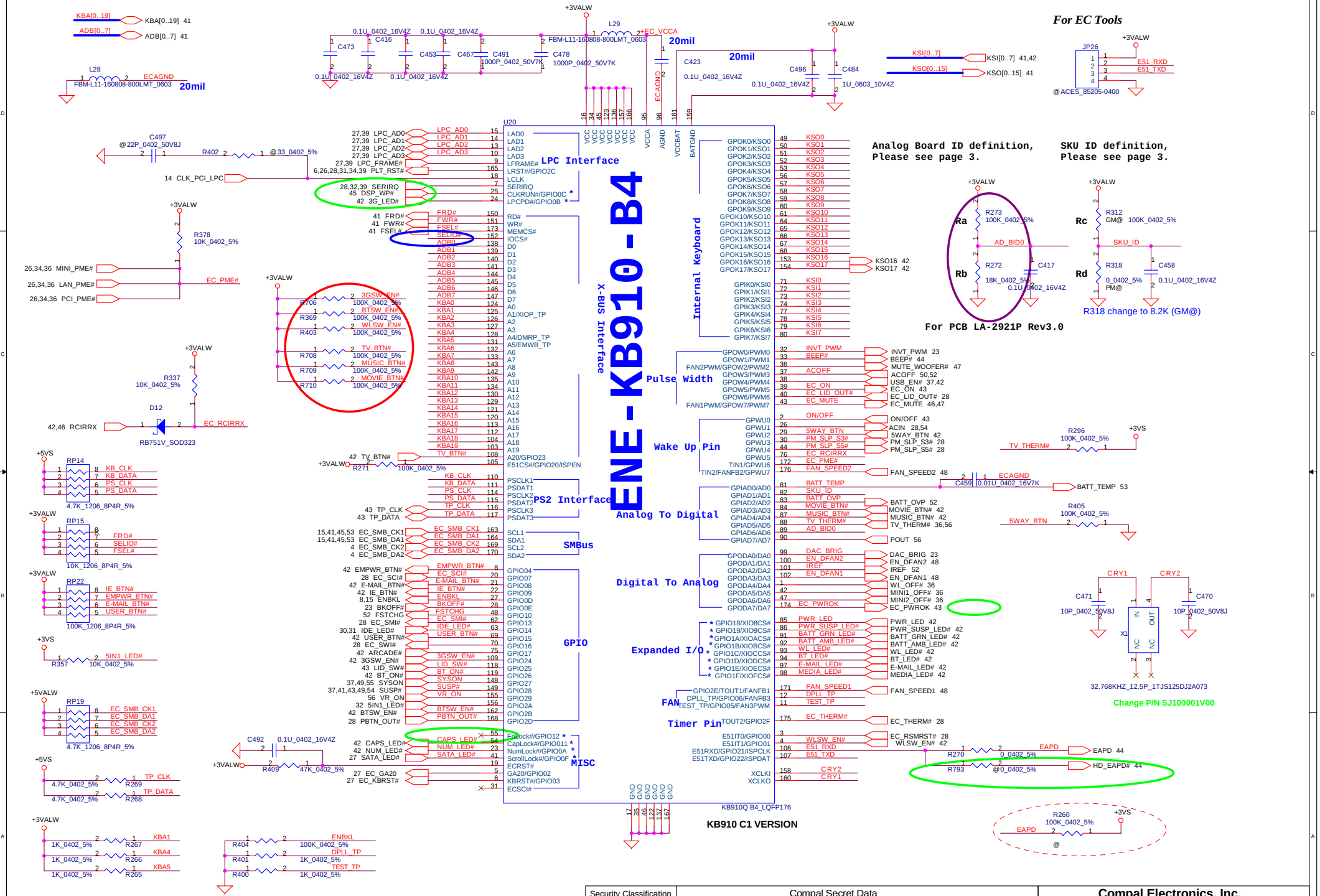

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Compal Electronics, Inc.

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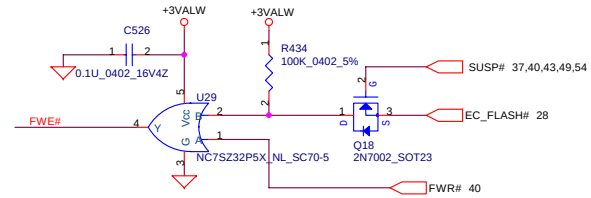
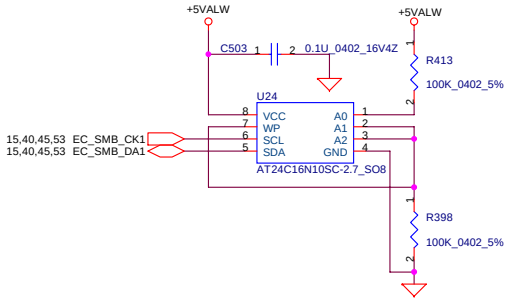
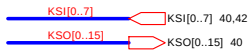
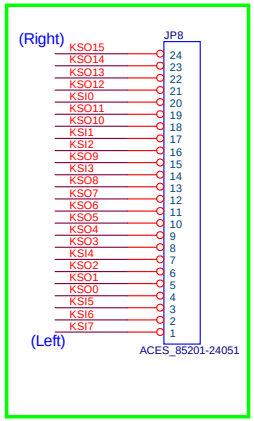


Check PCB Footprint

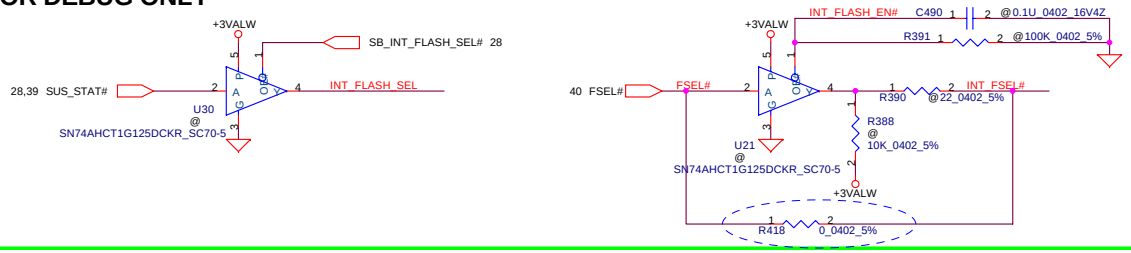


INT_KBD Conn.

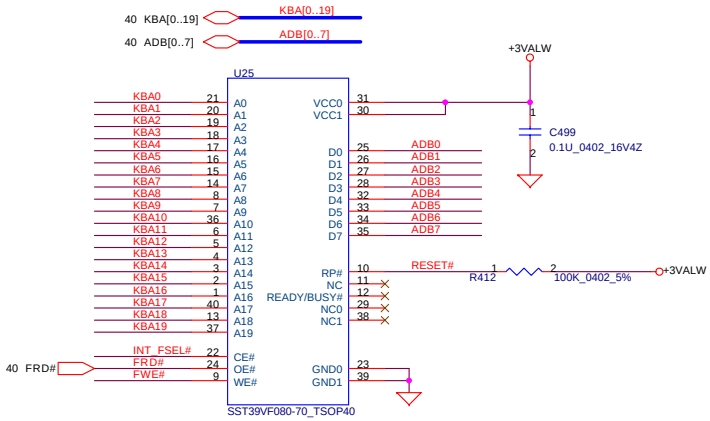




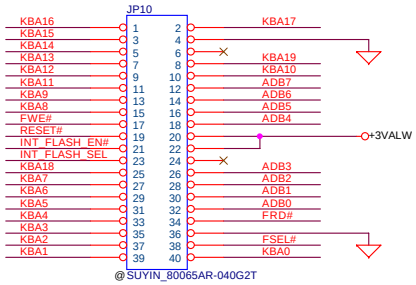
FOR DEBUG ONLY

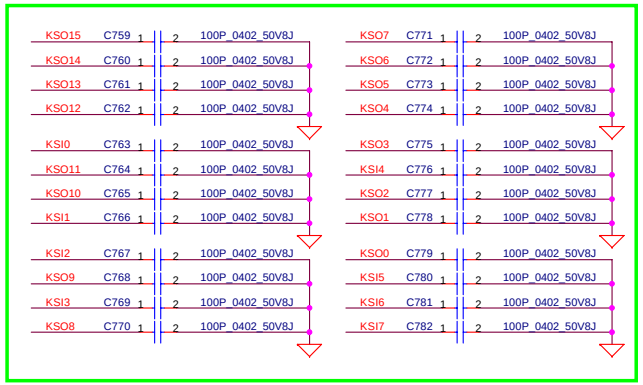


1MB Flash ROM



1MB ROM Socket





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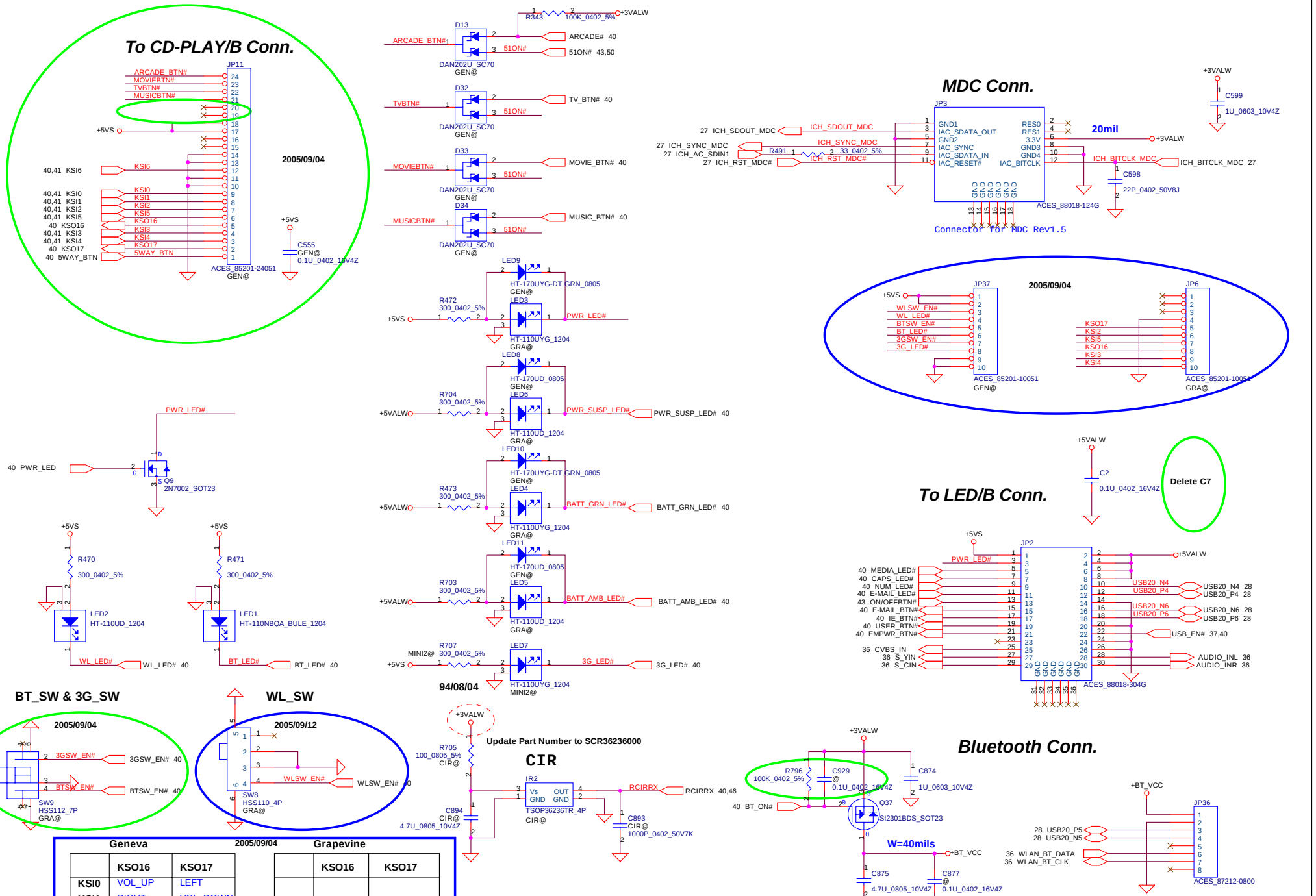

Geneva 2005/09/04

	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	
KSI4	NEXT	
KSI5	REV	
KSI6		RECORD

Grapevine

	KSO16	KSO17
KSI2	PLAY	
KSI3	STOP	VOL_UP
KSI4	NEXT	VOL_DOWN
KSI5	REV	ARCADE_TV

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Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

ON/OFF switch

Power Button

TOP Side
J2 @JOPEN
J1 @JOPEN
Bottom Side

+3VALW
R399 100K_0402_5%
D14 DAN202U_SC70
42 ON/OFFBTN# — ON/OFFBTN#
ON/OFF 40
51ON# — 51ON# 42,50
C495 1000P_0402_50V7K
D15 RLZ20A_LL34
40 EC_ON — EC_ON
Q16 2N7002_SOT23
R414 10K_0402_5%

Lid Switch

Change P/N : SN111000207
SW1 MPU-101-81_4P
2005/09/04
+3VALW
R8 100K_0402_5%
LID_SW# 40
D3 @ PSOT24C_SOT23

RTC Battery

BATT1
45@RTCBATT
+RTCBATT
D30 BAS40-04_SOT23
+RTCVCC
CHGRTC
C833 0.1U_0402_16V4Z

Scroll Up

SW2 EVQPLHA15_4P
SCRL_U

Scroll Left

SW5 EVQPLHA15_4P
SCRL_L

Scroll Right

SW6 EVQPLHA15_4P
SCRL_R
SCRL_R
BTN_R
D17 @ PSOT24C_SOT23

Scroll Down

SW7 EVQPLHA15_4P
SCRL_D
SCRL_L
SCRL_U
D19 @ PSOT24C_SOT23

Left

SW3 EVQPLHA15_4P
BTN_L

Right

SW4 EVQPLHA15_4P
BTN_R
SCRL_D
BTN_L
D18 @ PSOT24C_SOT23

Power ON Circuit

Change P/N : SA00000LR00

2005/10/20
+3VS
R420 180K_0402_5%
49,53,54 SUSP
Q41 2N7002_SOT23
C512 1U_0805_25V4Z
+3VALW
U28A SN74LVC14APWLE_TSSOP14
+3VALW POWER
U28B SN74LVC14APWLE_TSSOP14
R789 @0_0402_5%
SYS_PWROK 6,28
For South Bridge
40 EC_PWROK
R790 0_0402_5%
2005/10/20

2005/10/20
D36 RB751V_SOD323
R425 62K_0402_1%
C521 0.1U_0402_16V4Z
U28C SN74LVC14APWLE_TSSOP14
U28D SN74LVC14APWLE_TSSOP14
VS_ON 55
For +VCCP/+1.05VS

2005/10/20
R422 PM@ 62K_0402_1%
37,40,41,49,54 SUSP#
D37 RB751V_SOD323 PM@
C513 PM@ 0.1U_0402_16V4Z
C511 0.1U_0402_16V4Z
U28E SN74LVC14APWLE_TSSOP14
U28F SN74LVC14APWLE_TSSOP14
VGA_ON 57

To TP/B Conn.

+5VS
C176 0.1U_0402_16V4Z
40 TP_DATA
40 TP_CLK
JP7 ACES_87151-1207

BTN_R	C168	@100P_0402_50V8J
SCRL_R	C169	@100P_0402_50V8J
SCRL_U	C170	@100P_0402_50V8J
SCRL_L	C158	@100P_0402_50V8J
SCRL_D	C166	@100P_0402_50V8J
BTN_L	C173	@100P_0402_50V8J
TP_DATA	C167	@100P_0402_50V8J
TP_CLK	C159	@100P_0402_50V8J

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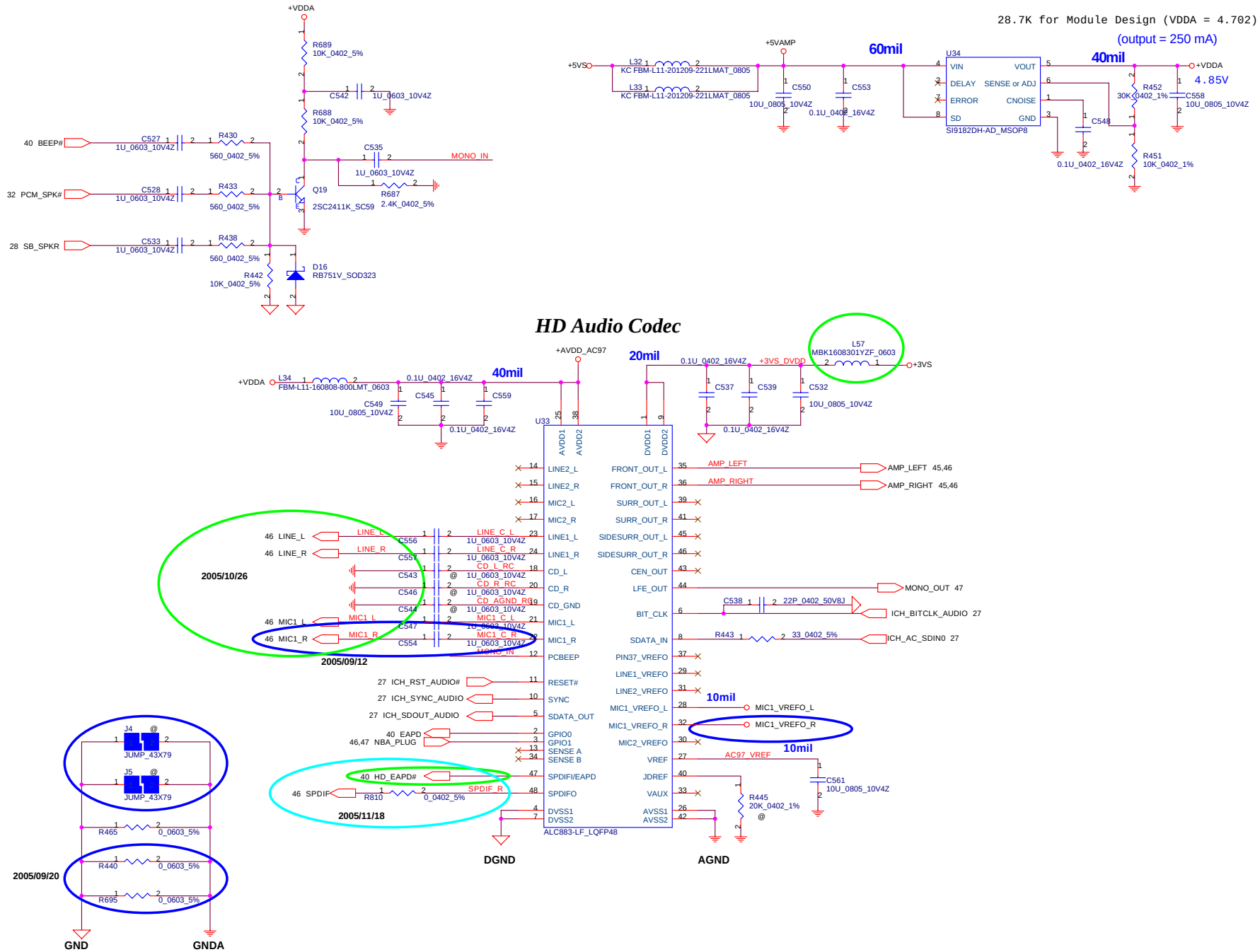

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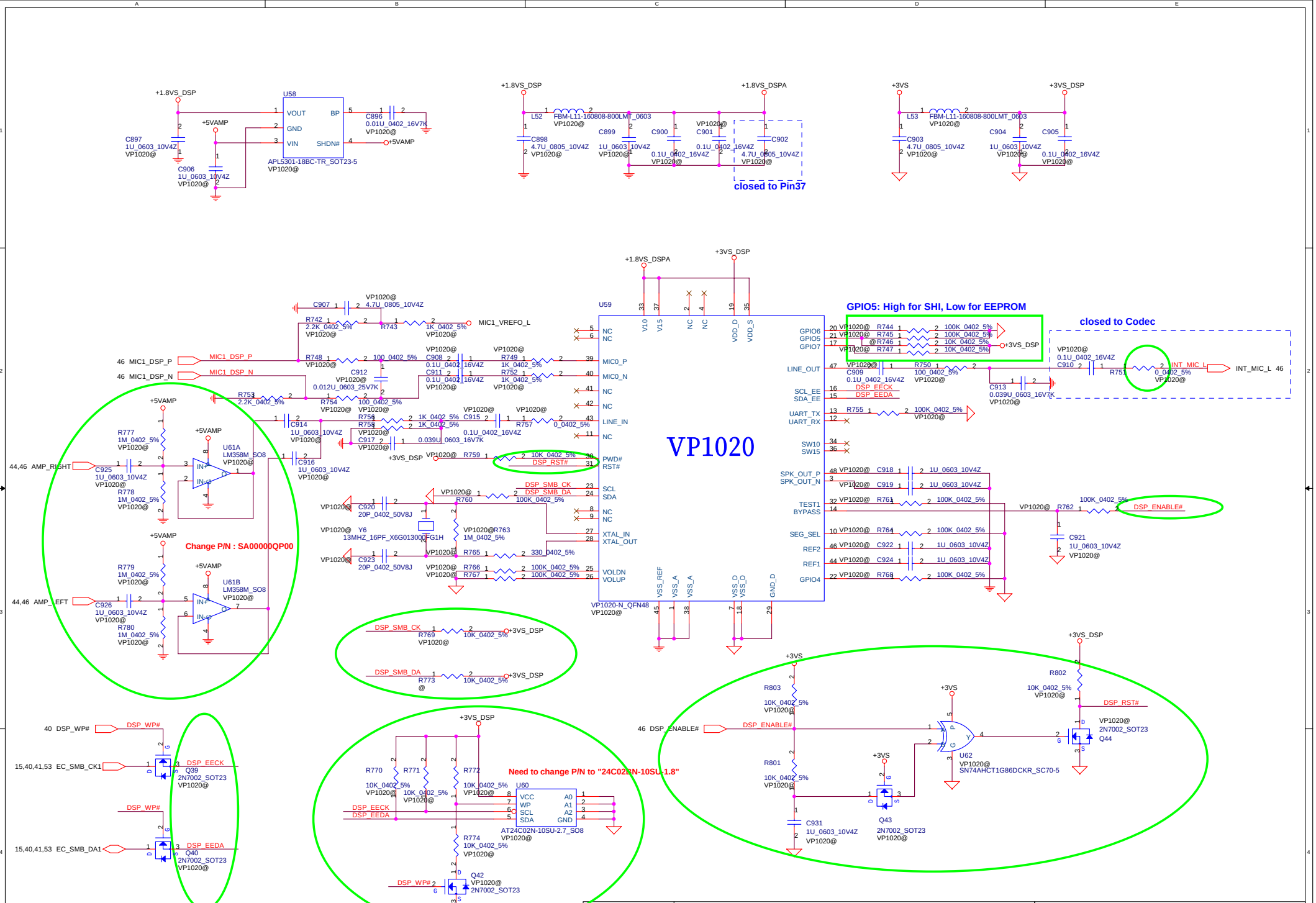

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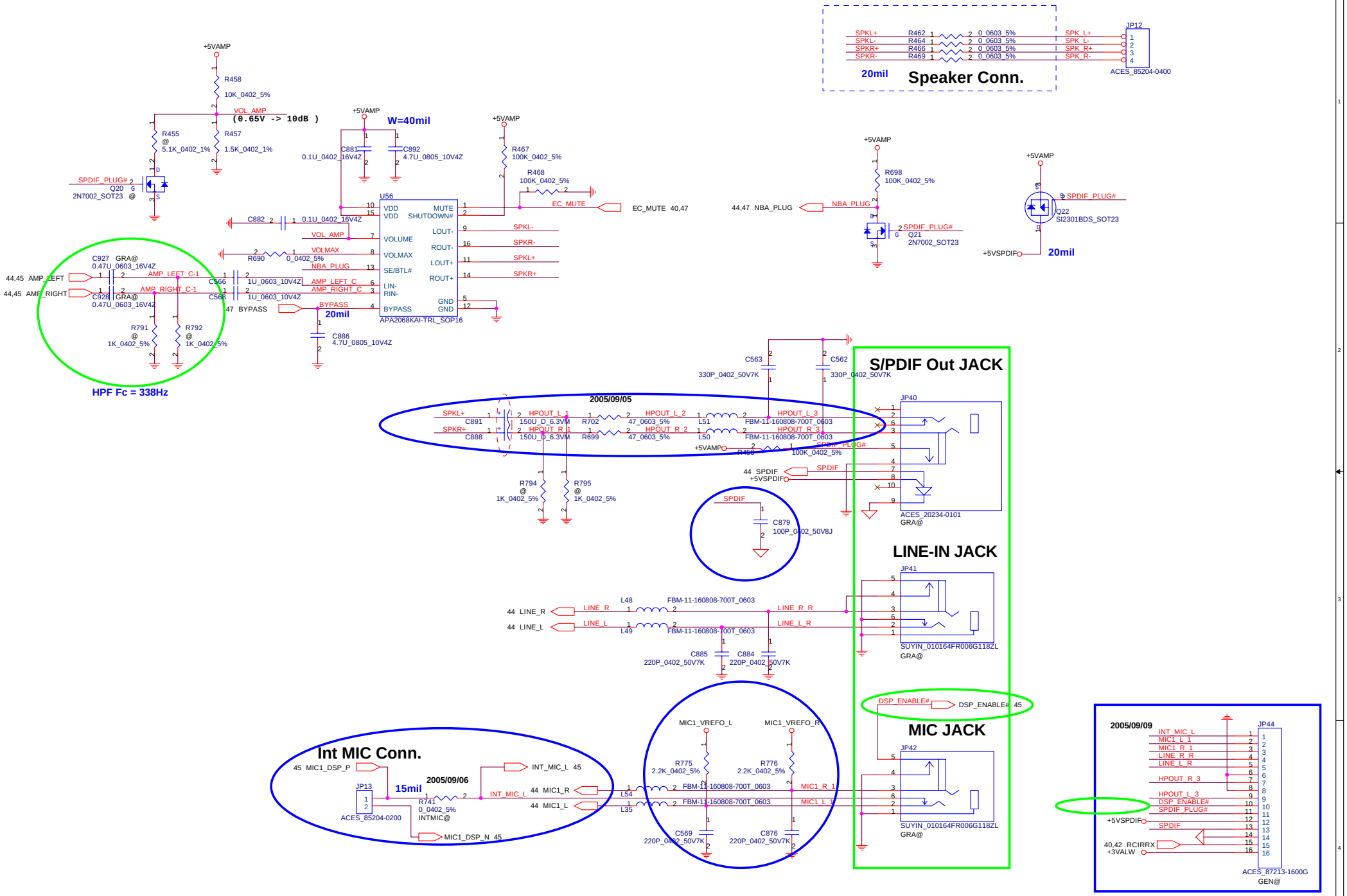

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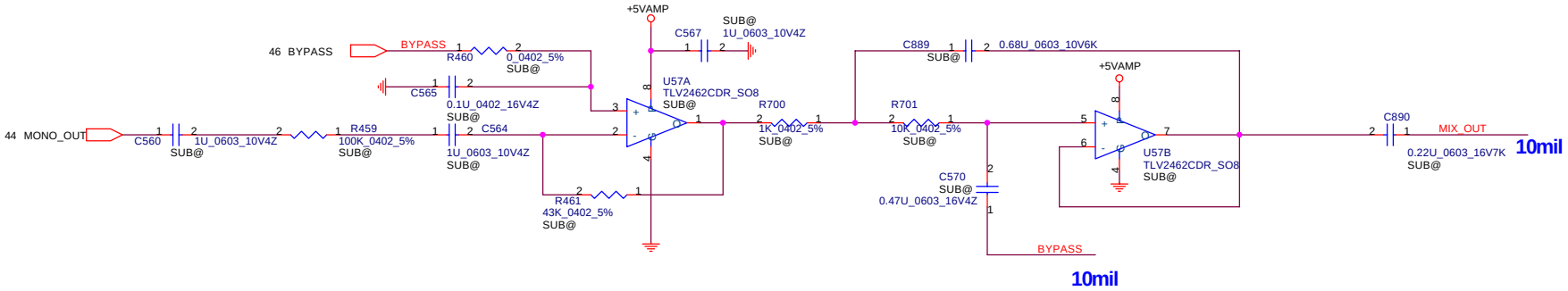
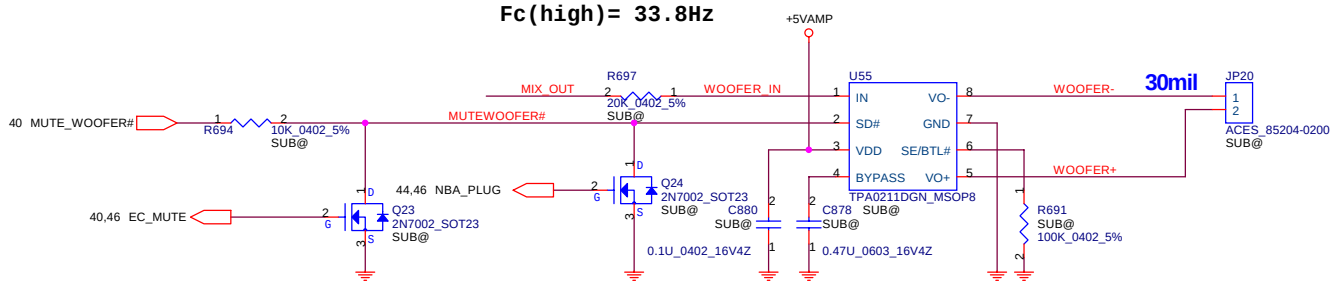


fo= 725 Hz

Fc(high)= 33.8Hz



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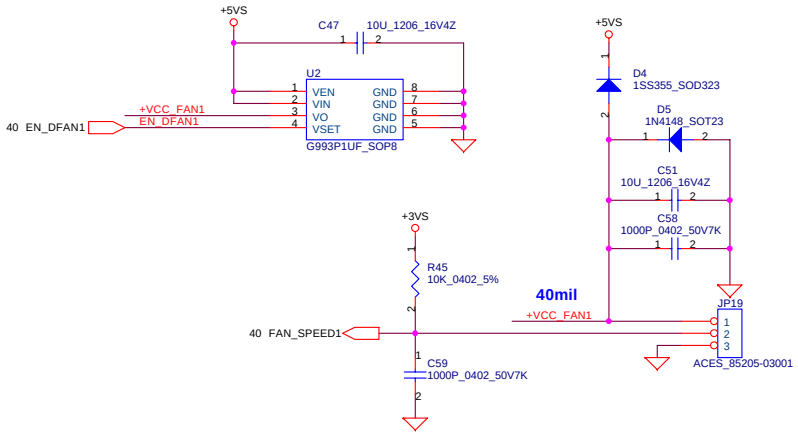
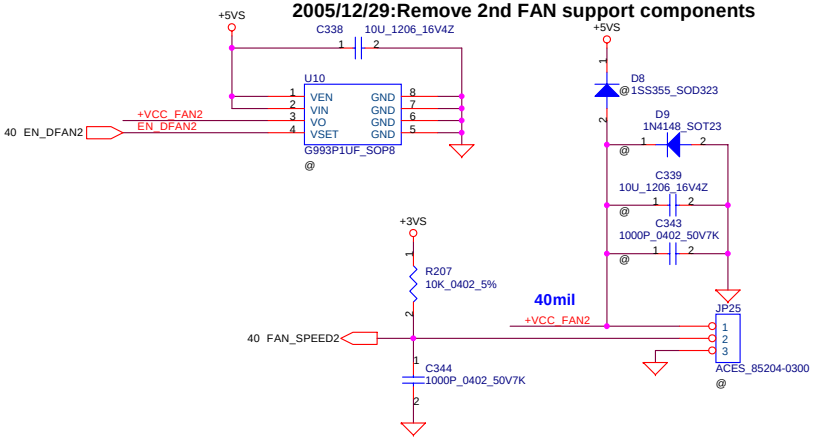
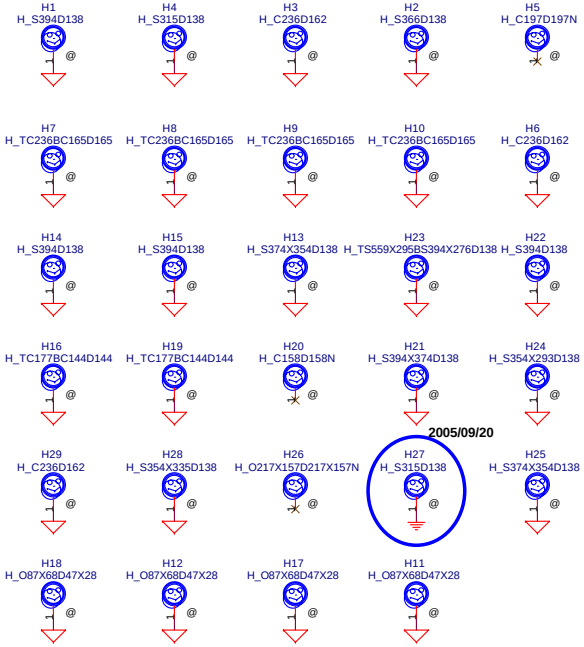
FAN1 Conn

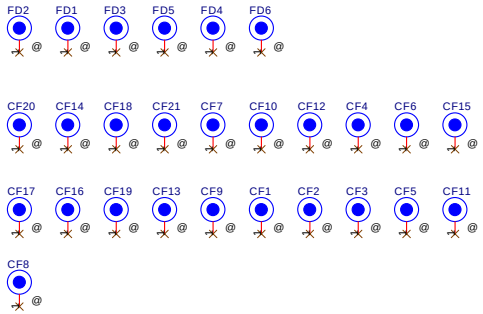


FAN2 Conn

2005/12/29:Remove 2nd FAN support components







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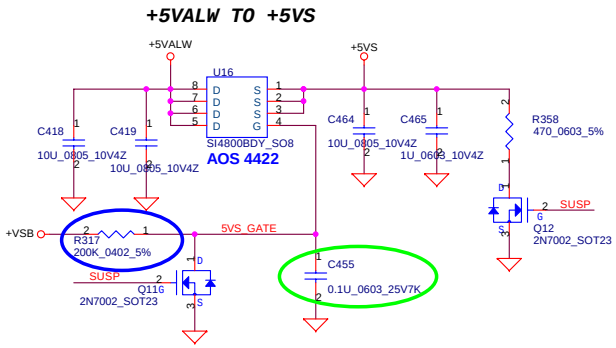
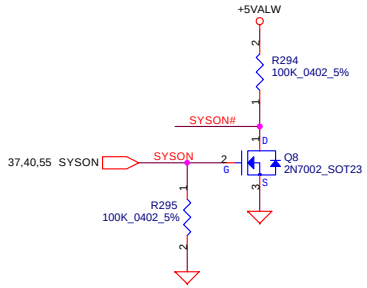
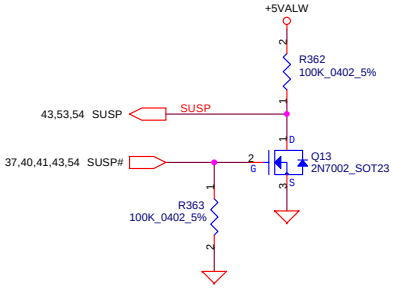
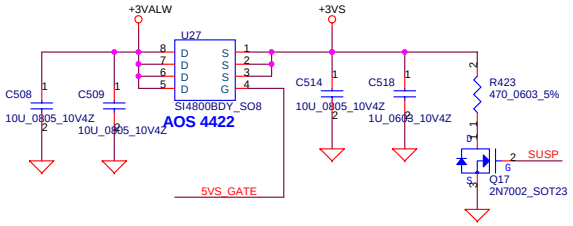
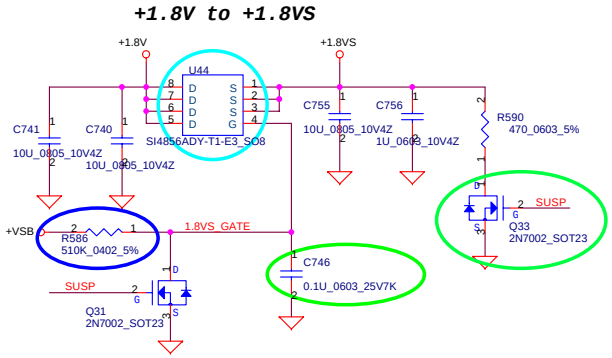


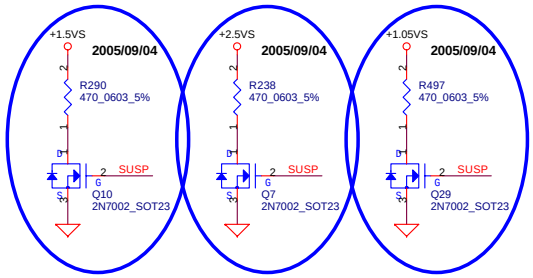


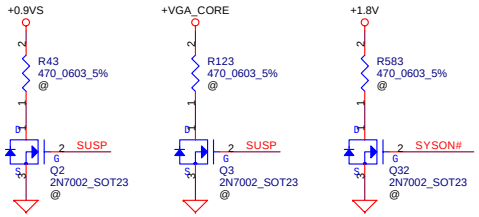




2005/12/18
Change P/N : SB000001Y00(New) SI4856ADY
SB548000310(Old)







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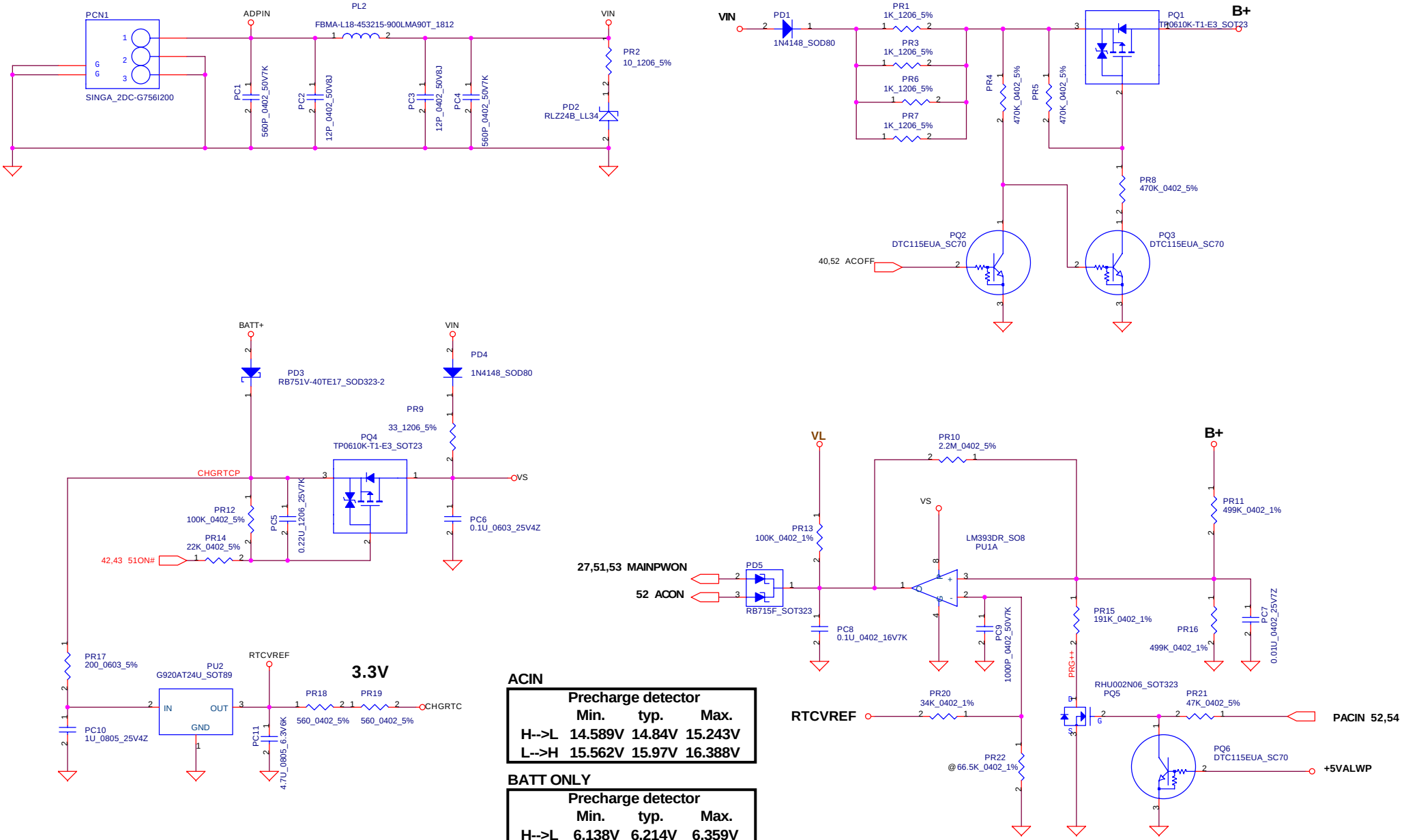

ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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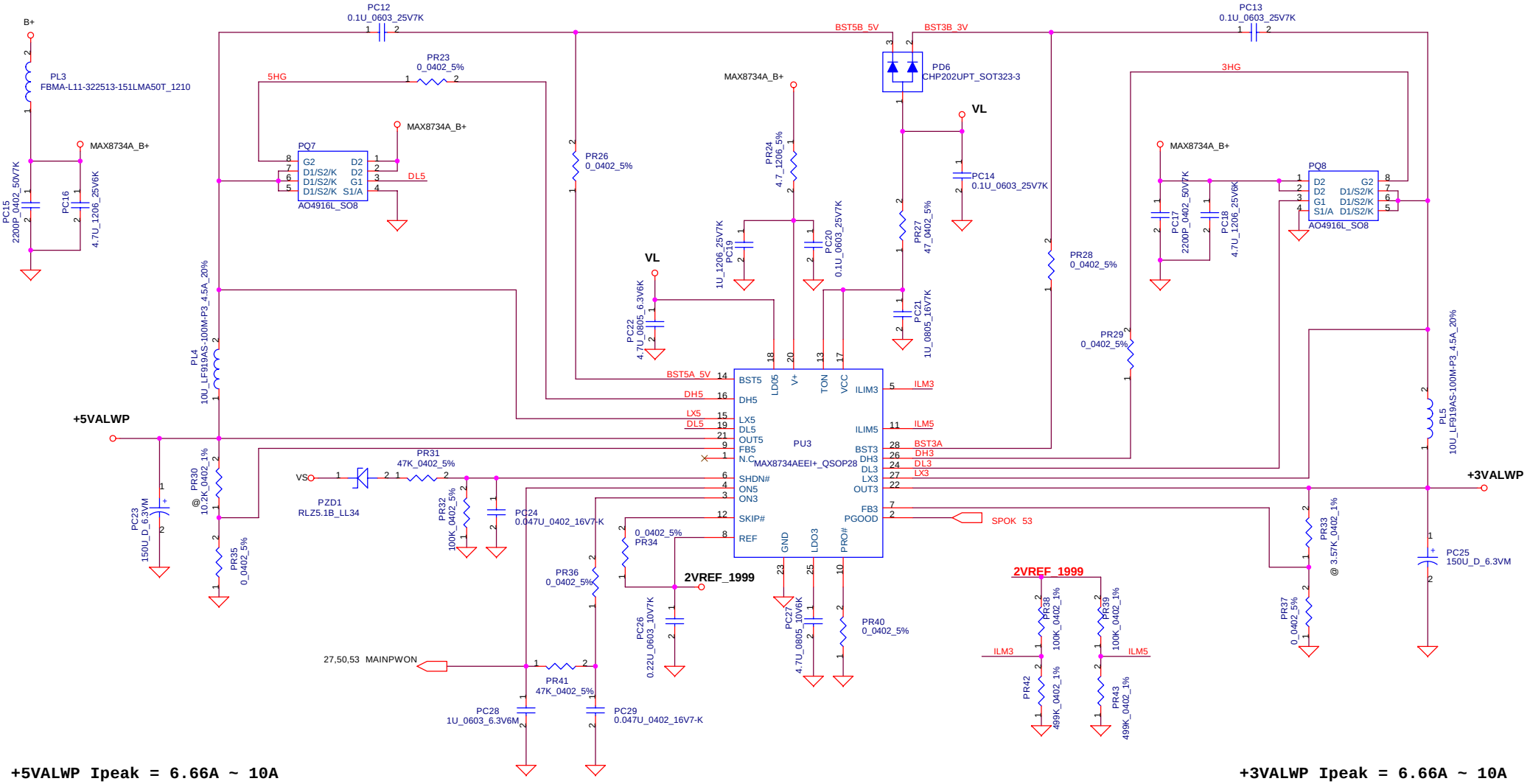

+5VALWP Ipeak = 6.66A ~ 10A

+3VALWP Ipeak = 6.66A ~ 10A

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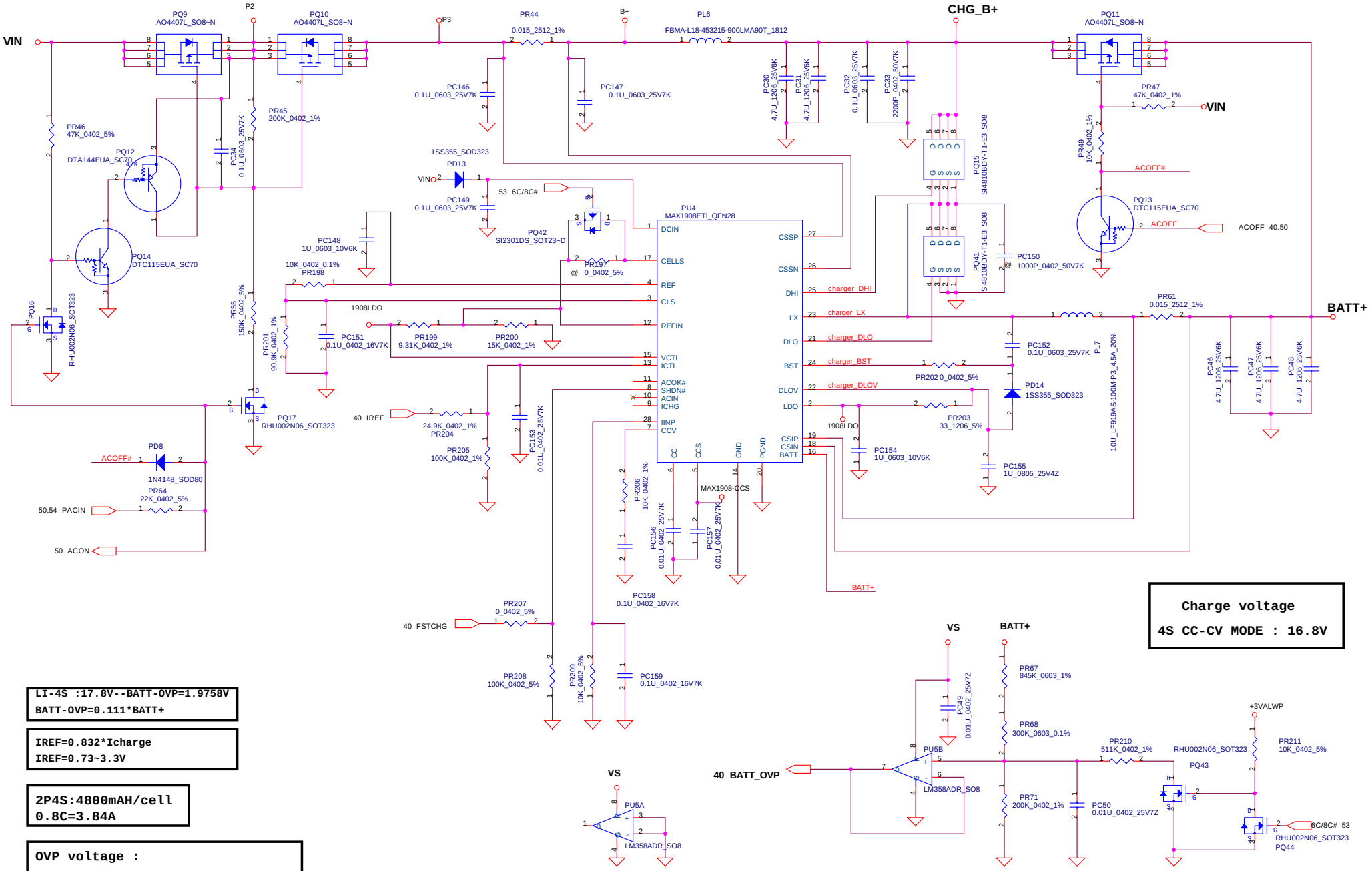
Charger

Iadp=0~4.74A(90W)



Charge voltage

4S CC-CV MODE : 16.8V

LI-4S :17.8V--BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

IREF=0.832*Icharge
IREF=0.73~3.3V

2P4S:4800mAH/cell
0.8C=3.84A

OVP voltage :

LI-3S :17.8V----BATT-OVP=1.9758V

BATT-OVP=0.111*BATT+

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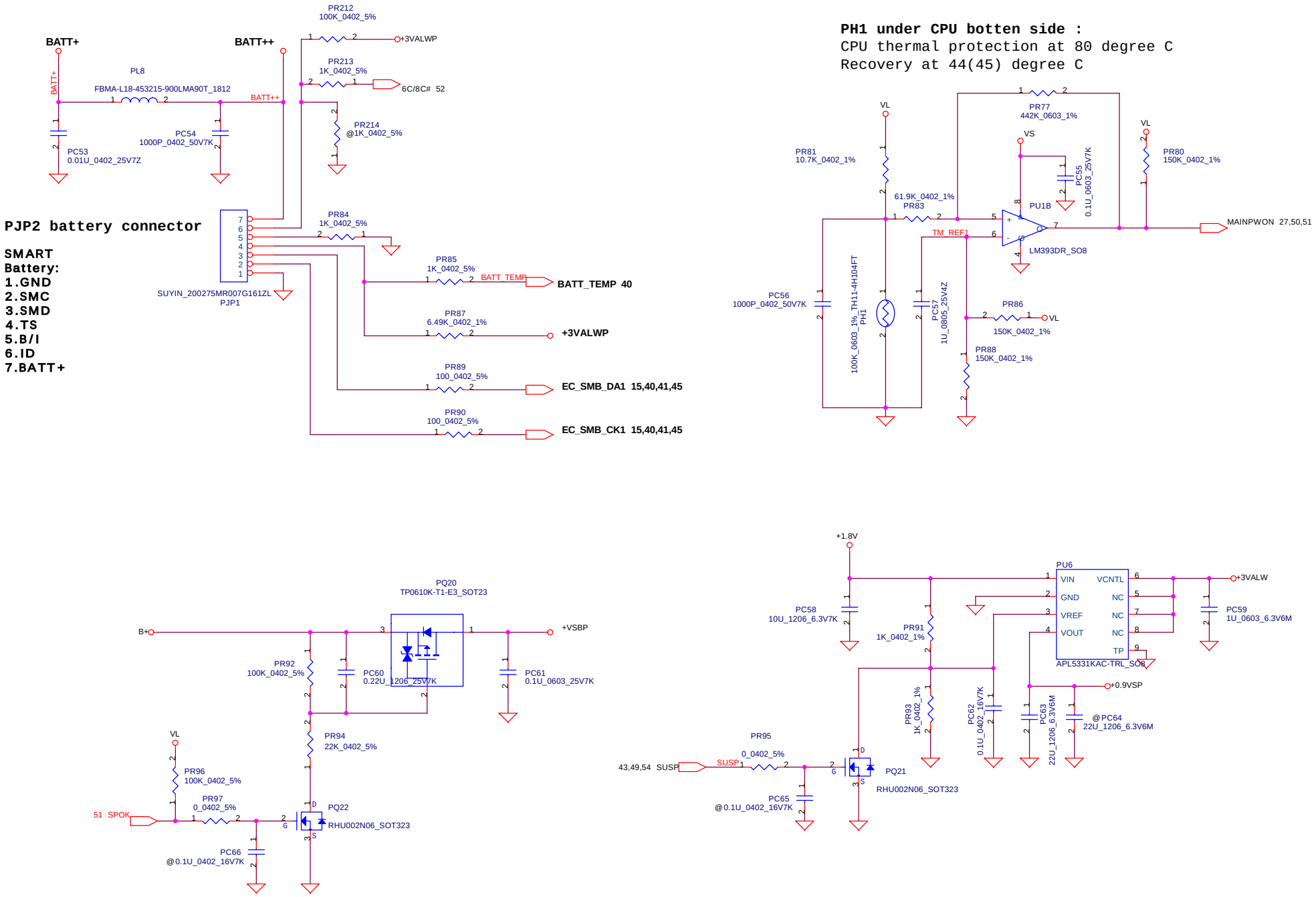

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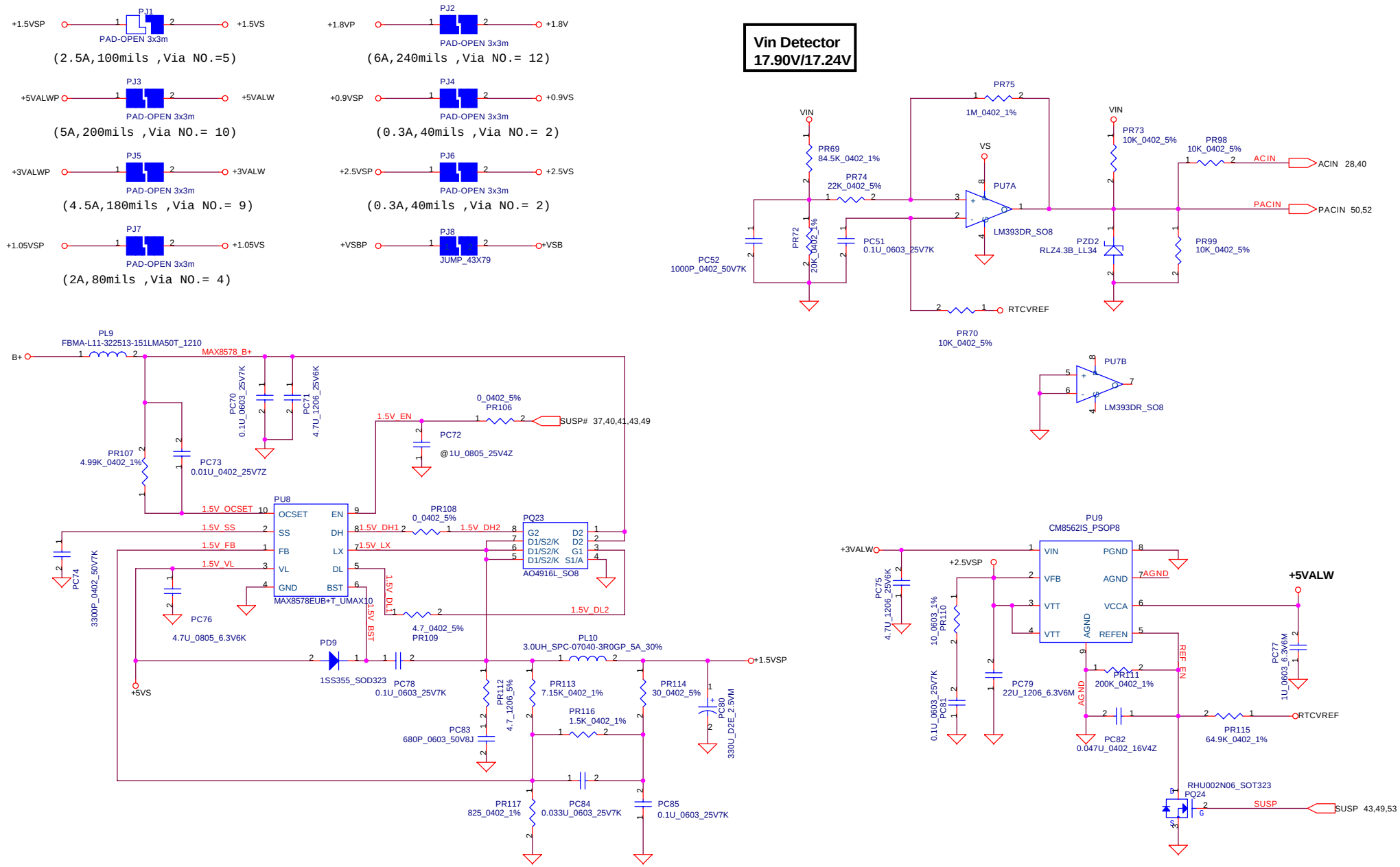
AC Adapter Detector



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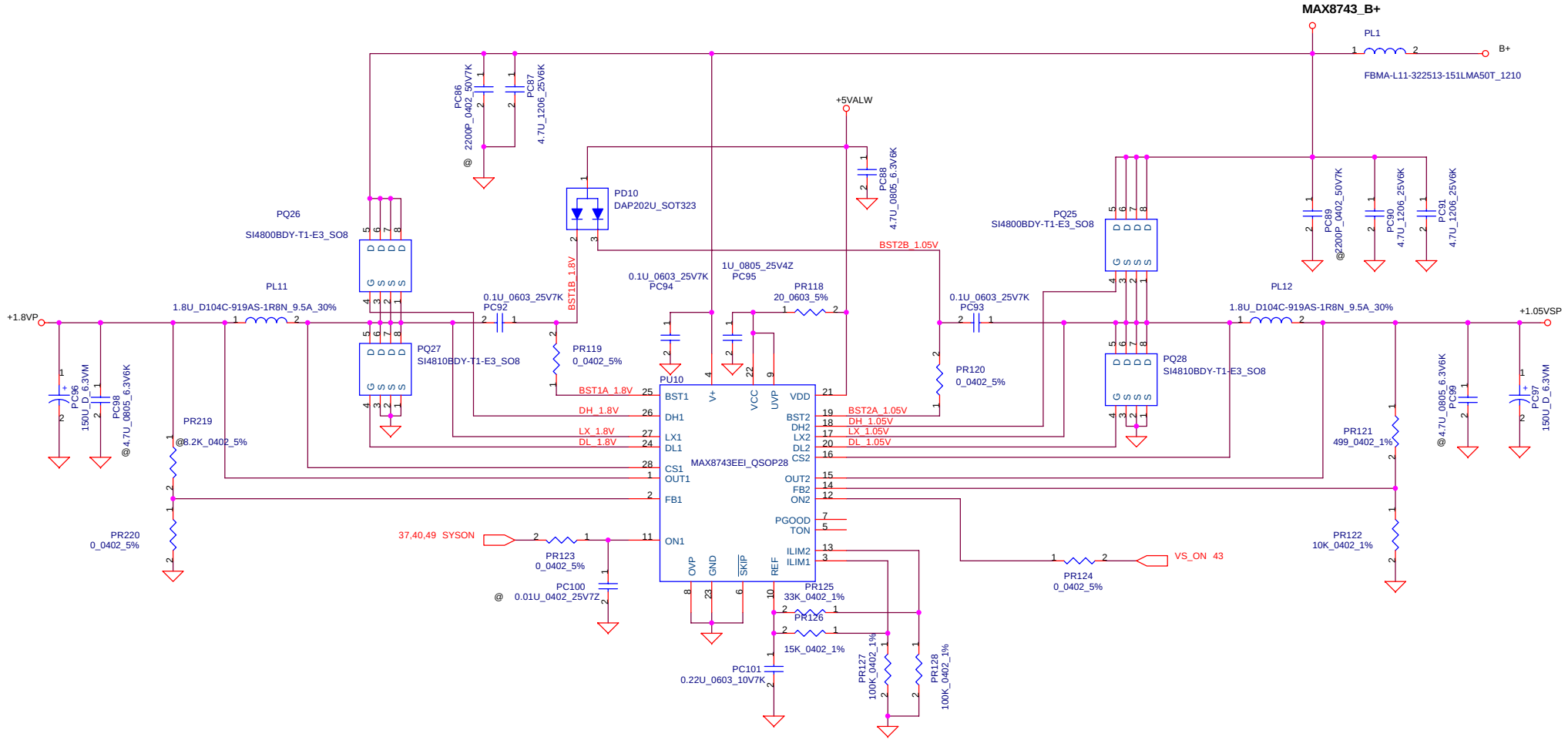

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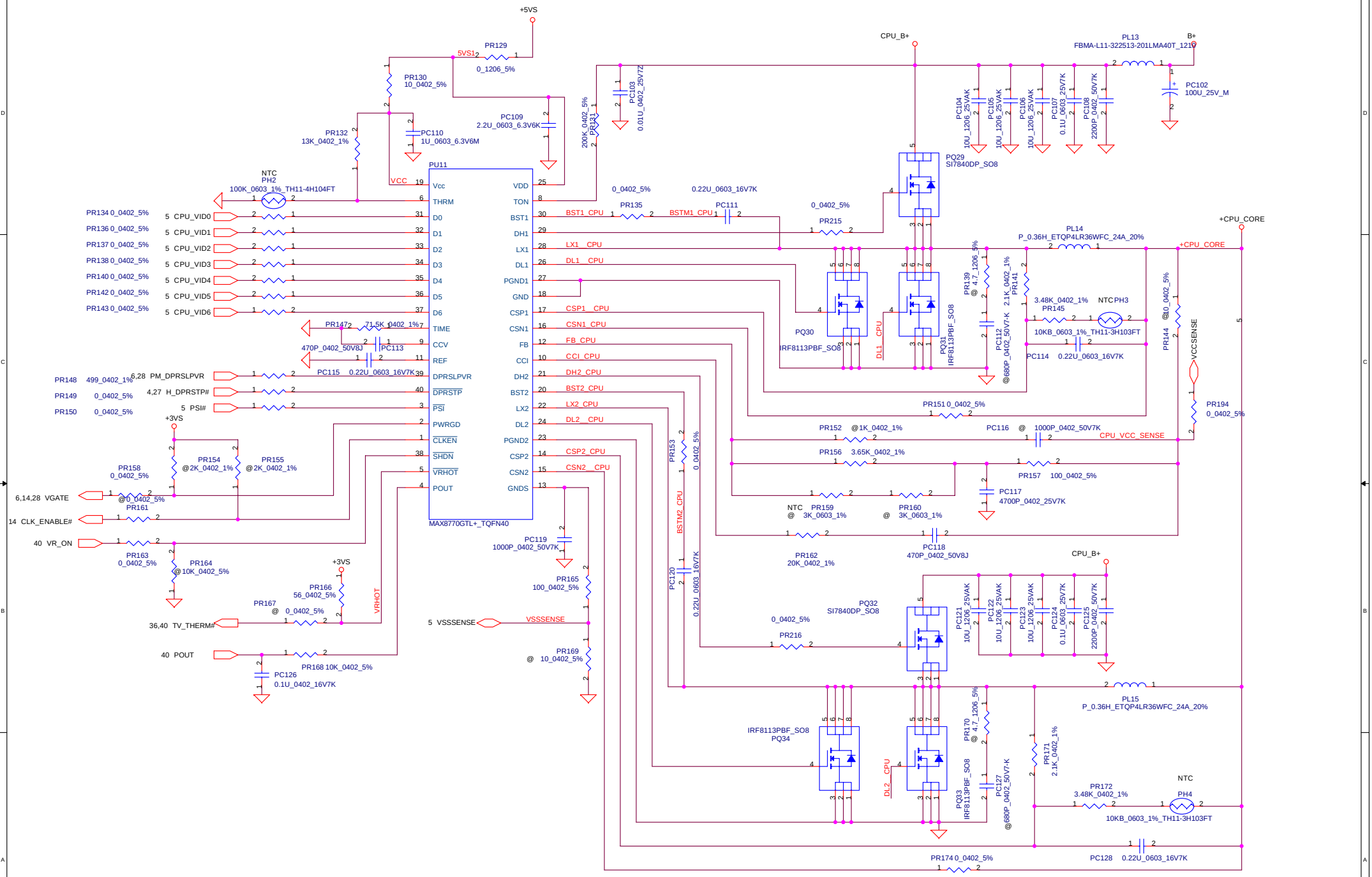

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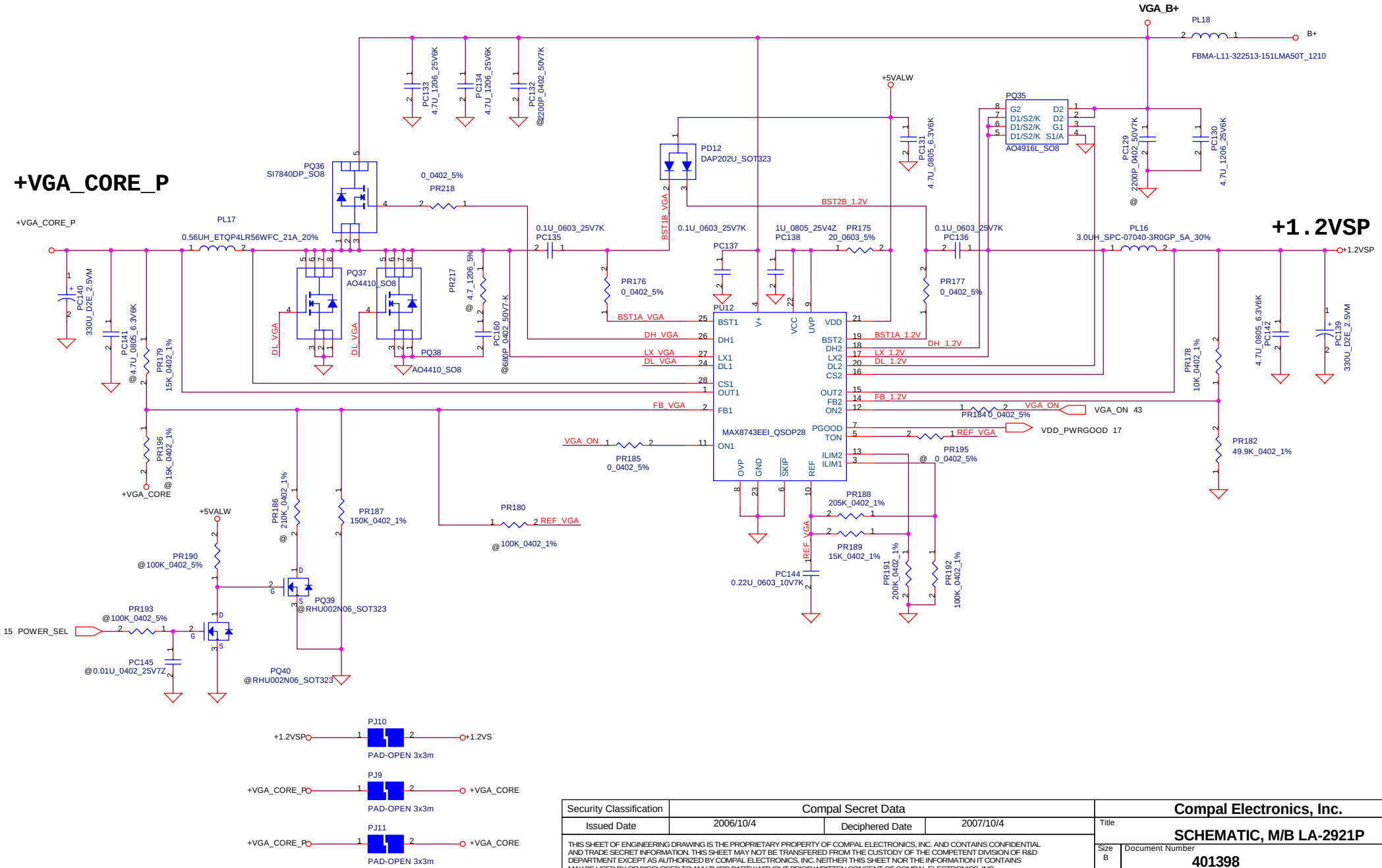
POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



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A --> B Change List

1. Page06 : No stuff R100 10K_0402_5%
2. Page09 : Add C49 & C887 220U_D2_4VM
3. Page10 : No stuff R57 2.2K_0402_5%
4. Page14 : Add R711 10K_0402_5% to set 96MHz output
   Change Q14 & Q15 pin1 net name to connect to ICH7M
   Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P_0402_50V8J to 18P_0402_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA_DDC_CLK & VGA_DDC_DATA to Q26 & Q27 Level shift.
   Add R781 & R782 4.7K_0402_5%
   Change C589, C596, C583, C587, C594, C585 to 150P_0402_50V8J
8. Page28 : Change SB_INT_FLASH_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U_0402_16V4Z to 1U_0402_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R_0402 (0_0402_5%)
11. Page34 : Stuff R175 & no stuff R182(0_0402_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN_ACTIVITY# & LAN_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.
    Swap JP17 PCIE TX & RX Signal.
    Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M
    Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394@ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.
    No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.
    Change SW8 & SW9.
    Add JP37.
18. Page43 : Change U28 Part Number.
    Change SW1 Part Number.
    Change R425 from 10K_0402_5% to 62K_0402_1%
    Change R422 from 10K_0402_5% to 62K_0402_1% & add C513 0.1U_0402_16V4Z
19. Page44 : Add C554 for MIC_R
    Add R440, R695 (0_0603_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.
    Reserved C879 for EMI request
    Modify MIC Jack circuit. add R741, R775, R776, L54, C876
    Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29
    Change R317 to 200K_0402_5%
    Change R586 to 510K_0402_5%

B --> C Change List

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K_0402_5% to 10K_0402_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA_CORE
6. Page18 : Modify PEX_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing
   Modify SATA HDD connector library
8. Page31 : Delete IDE_CD_L, IDE_CD_R & CD_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,
   Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC_PWROK, reserved Q41, R420, C512
    add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

Rev0.3 --> Rev0.4 Change List

1. Page15 : Add R809
2. Page23 : Reserved C934, C935, C936 for EMI
3. Page26 : Add U51, R811, Reserved R330
4. Page44 : Add R810 for EMI.

2005-12-19

1. Page 48: Delete 2nd Fan support components U10, D8, D9, C339, C343, JP25

2006-01-04

1. Page 16: Update VRAM Infineon strap setting.

2006-01-23

1. Change U42 part number from SA00000QZ00 to SA00000QZ10
2. Update C877 to no-stuff.

2006-02-06

1. Update R148 note as 30.1_0402_1% for G72MV & 40.2_0402_1% for G73M. (Not apply wait Nvidia document)

2006-03-02

1. Modify Camera power from +5VS to +3VS.
2. Add HDCP function. (U67, R818, R819, C946)

2006-03-28

1. Add R212 with 5787@ BOM Structure property at Page 34 for S5 wake up function of BCM5787M.

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